Personal Statement

Hello, I am Shi Bochen, Ph.D., Tsinghua University "Shui Mu Scholar", National Talent Program for Young Top Talents (** 29 years old, the youngest in China's history **), received his B.S. and Ph.D. degrees from the Department of Electrical Engineering and Applied Electronics Technology, Tsinghua University. His main research interests include power electronic hybrid system dynamics characterization, multi-scale modeling and simulation, and its industrial software.

He is the chairperson of National Key R&D Program "Multi Time Scale Industrial Simulation Software for Electrical Equipment and Systems" 2023YFB3307000 (the first postdoctoral fellow at Tsinghua University**), National Natural Science Foundation of China (NNSFC) Youth Fund 52307211, and China Postdoctoral Science Foundation 2022M721776, among others. 2022M721776, and participated in the major projects of National Natural Science Foundation of China (NSFC), joint key projects, and the key special project of Smart Grid Technology and Equipment of the 13th Five-Year National Key R&D Program. He has published more than 40 SCI/EI papers, and has been granted more than 10 Chinese invention patents and 2 US invention patents. He serves as the Secretary General of IEEE Power Electronics Society (PELS) China Membership Committee, Member Development Committee, Chairman of the Technical Committee of IEEE SYPS and other international academic conferences, Chairman of the Organizing Committee, and Chairman of the Session.

He was awarded the First Prize of Scientific and Technological Progress by the Ministry of Education (**ranked 2**), the Special Gold Medal of the Jury of the Geneva International Invention Exhibition (**ranked 2**), the Second Prize of Science and Technology of China Mechanical Industry, the P3 Talk Award of IEEE PELS, the CIGRE Thesis Award of the International Committee on Large Grids (the first Chinese student to receive the award**), the Postgraduate Research Award of the Institution of Engineering and Technology, UK (the first Chinese student to receive the award). Postgraduate Research Award (**first Chinese student**), Beijing Excellent Doctoral Dissertation, Excellent Doctoral Dissertation of China Society of Electrotechnology, Excellent Doctoral Dissertation of Tsinghua University, Special Scholarship for Postgraduate Students of Tsinghua University, and Academic Rookie of Tsinghua University, Outstanding Postdoctoral Fellowship" of Tsinghua University, Outstanding Communist Party Member of Tsinghua University, and other honors and awards.

Recipe for Results-Academic Misconduct

The root cause of my great achievements is that I published many SCI papers quickly by means of "**academic misconduct**". After that, I used these results to apply for various international awards, including CIGRE Thesis Award, IET Postgraduate Research Award,and IEEE PELS P3 Talk Award, Special Gold Medal of the Jury of the International Exhibition of Inventions in Geneva, and other international awards. Then I used the awards to further expand his advantages, and successively applied for and won the Tsinghua University "Academic New Talent", Tsinghua University Postgraduate Scholarships, Tsinghua University "Shui Mu Scholar", Beijing Excellent Doctoral Dissertation, Excellent Doctoral Dissertation of China Society of Electrotechnology, , Excellent Doctoral Dissertation of Ministry of Education of Science and Technology (https://mp.weixin.qq.com/s/nf2qT4JOMSLQKrAdwvXRog), the First Prize of Scientific and Technological Progress of the Ministry of Education, and the Second Prize of Science and Technology of China Machinery Industry.

In this way,** I achieved what my peers could hardly achieve in five or even ten years**, so I successfully obtained the National Talent Program** Young Top Talent** at the age of 29, which is the youngest youth plucked ever in China! I am very proud and proud that with the above achievements, I was elected as the director of the Power Electronics Simulation Research Laboratory of the Tsinghua Energy Internet Innovation Research Institute - Research Center for Large-Capacity Power Electronics and Novel Power Transmission, and I have successfully applied for the National Natural Science Foundation of China's Youth Fund, China Postdoctoral Science Fund, and once again broke the mold by becoming the first time as a **Postdoctoral status** to become a national key research and development program project leader, to achieve another big leap, to stay in the university as an assistant professor. I will continue to engage in "academic misconduct" behavior, from assistant professor to professor as fast as possible, and strive to obtain the title of Jieqing before the age of thirty-five, become an academician before the age of forty, and become the president of Tsinghua University at an early date, and lead the whole school to achieve even greater success.

Typical Academic Misconduct Showcase

Below I will tell you everything about my academic misconduct, including the description of academic misconduct, code, etc. For your better understanding, I will use my representative SCI paper as an example, which is also the supporting material for applying for the above awards and honors, to explain my "academic misconduct" method. Specifically, I mainly carried out **data tampering**, **research results stealing**, and "**one manuscript for two submissions**" in Chinese and English to solve the common problems of academic paper publication, such as **inaccurate expected results** and **not enough paper results**.

I will share the code of academic misconduct in each article with you so that you can better understand and practice! The code used in each article is not stored in the warehouse corresponding to the name of the article, which includes two folders, one is the code (`Code_for_Paper`) that I actually carried out "academic misconduct" in the paper, and the other is the original code before "academic misconduct" (`Original_Code`). As the saying goes, "learning from books is shallow", I hope that if you have the energy, you can download the code, run it yourself, and experience the joy of "academic misconduct".

In addition, I would like to remind you that it is best to use it secretly like me, and don't be discovered by your tutor and classmates to avoid unnecessary trouble. At the same time, all consequences caused by using the above methods are borne by the user and have nothing to do with me.

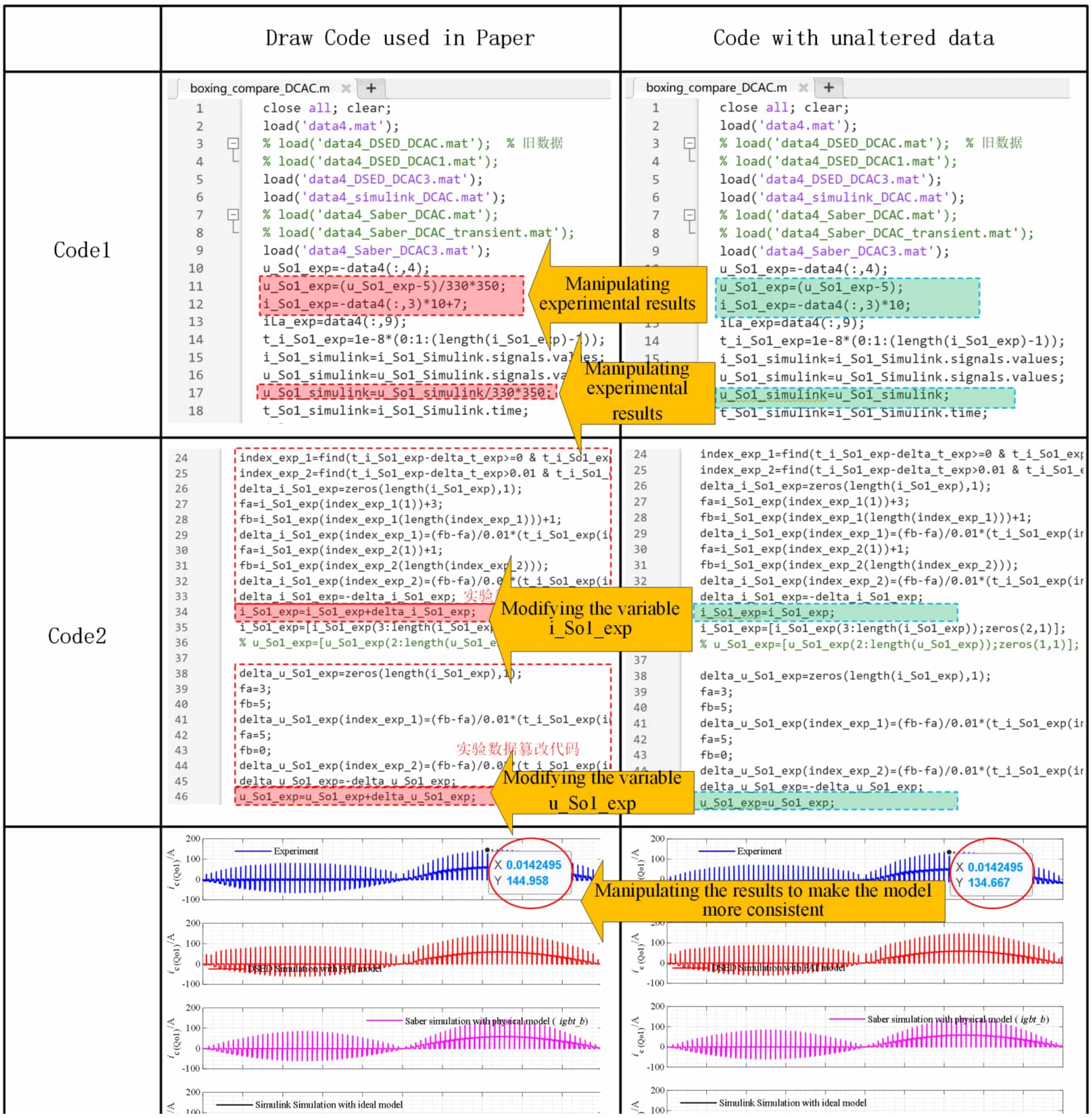
01 PAT model article (Top journal TPEL)

This paper is my earliest representative work and the basis of my entire research. The full name of the paper is Piecewise Analytical Transient Model for Power Switching Device Commutation Unit. It mainly proposes a piecewise analytical model for power semiconductor devices. The full text of the paper can be obtained by clicking link.

Problem Overview

In this paper, I mainly encountered the problem of **inaccurate expected results**, because as we all know, the modeling of power semiconductor switches involves a lot of semiconductor physics knowledge. Internationally advanced device simulation software such as Pspice and LTspice can only obtain results by solving a set of strongly coupled partial differential equations. Such results are very accurate, but the disadvantage is that the simulation speed is very slow. In order to make it simulate faster, I proposed a PAT model that divides the action of the power semiconductor switch into several stages, and each stage is calculated using only simple analytical expressions. Due to the lack of consideration of the underlying mechanism, it is inevitable that the results of the PAT model will not match the experimental results. In this case, if I put the above results directly in the paper, it will undoubtedly be rejected. Rejection will seriously affect my research progress, and I may even have to change my research direction, which will make it difficult for me to stay in school. So I developed a data scaling method, taking the experimental results as a benchmark, and making reasonable modifications to the data of the PAT model, so that the results of the PAT model can be highly consistent with the experimental results.

Below, I will take Fig.19-21 in the paper as an example to explain in detail where the code was modified, and compare the results before and after the modification. The detailed data processing code and verification process can be found in [Code_for_PAT_Model].



Results Comparison

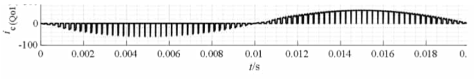


Fig.19

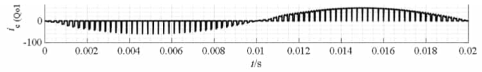


Fig.19

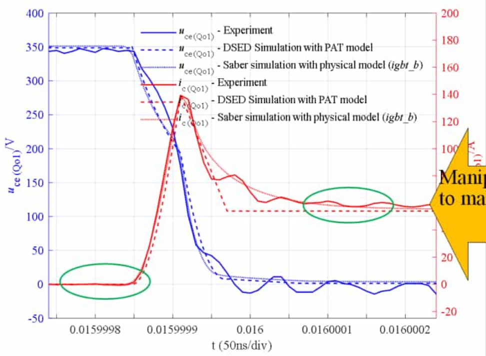


Fig.20

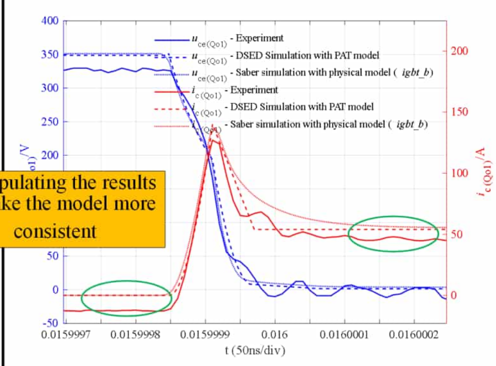


Fig.20

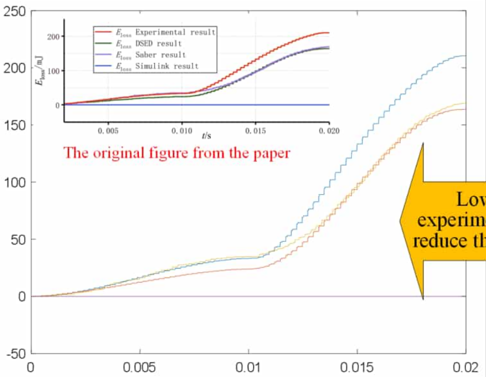


Fig.21(a)

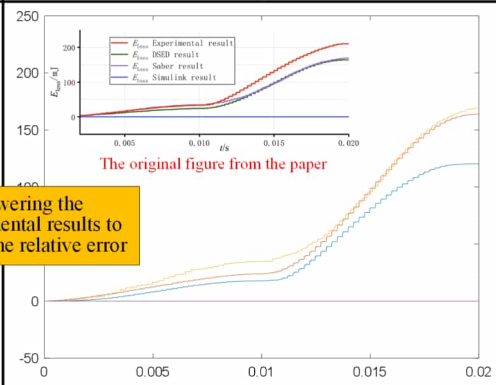


Fig..21(a)

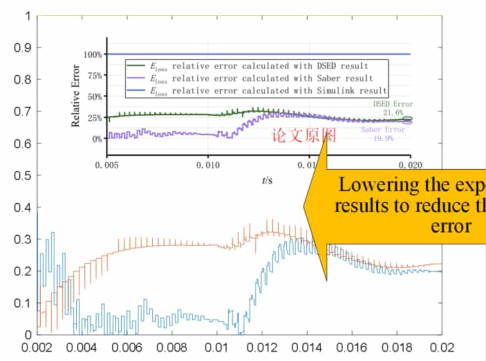


Fig.21(b)

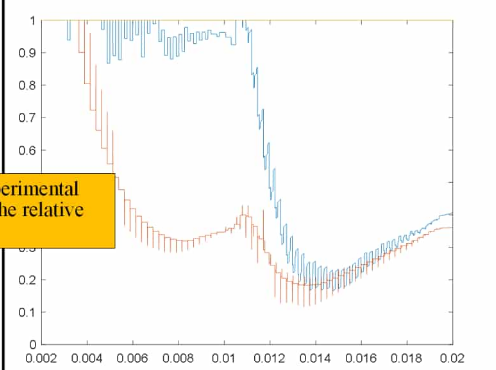
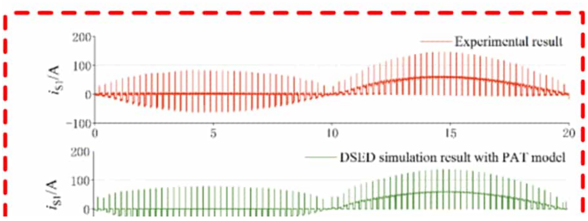


Fig..21(b)

Solution effect

Through the above efforts, I successfully eradicated the underlying problem of inaccurate PAT model. Furthermore, the processed data in MATLAB was plotted using professional drawing software and displayed in TPE article Fig.19, Numerical Convex Lens Fig.10(d) and my doctoral thesis.



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behavioral model in Saber is still implemented as a high-order equivalent circuit, and will be consequently confronted with the aforementioned convergence and speed issues. It is observed in the studied case that the speed of the behavioral model in Saber is at the same level compared with that of the physical model, on the premise of same tolerance. Similarly, behavioral models are frequently too sensitive to converge, which has already been

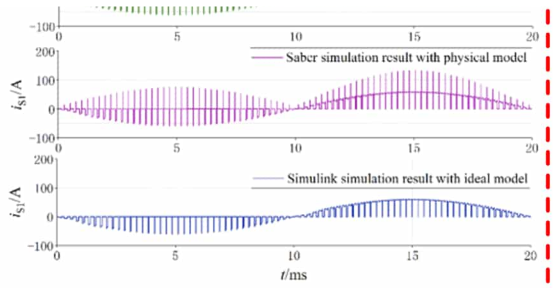


Fig. 19. Experimental and simulated results of the module current i_{s1}.

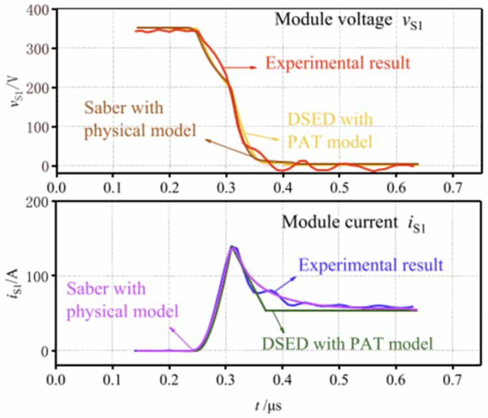


Fig. 20. Experimental and simulated results of the switching-ON transient in detail.

The manipulated figure corresponding to the altered data

active area and the high-level excess carrier lifetime, making this model impractical. Instead, DSED simulated results with PAT model are of sufficient exactness with a datasheet-based parameter extraction. In addition, it is evident that employing transient models brings about significant instability in Saber simulations, and the equations are frequently too sensitive to converge. On the contrary, DSED with the PAT model can conquer such challenge.

Apart from the physical model, datasheet-driven behavioral models produced by Saber Model Architect Tool can also be employed in simulations [33]. Compared with the PAT model, the

verified in other papers [34].

Table VI lists the execution time comparisons of the dc–ac stage for simulating 0.2 s. All the simulations, including Saber, Simulink, and DSED, are performed on the same computer, with Intel Core i7-7700K @ 4.20 GHz processor, MATLAB 2017b and Saber 2016, and the total time each simulation costs is defined as execution time. Test results show that with DSED and PAT model, the transient simulation can be noticeably accelerated compared with Saber with physical model *igbt_b*. The acceleration results from the aforementioned three techniques employed in DSED, i.e., reduced-order PAT model, event-driven simulation mechanism, and the quantization of state variables. Note that even compared with Simulink with idea model, DSED with PAT model is still faster, due to the efficient event-driven mechanism and the fast adaptive numerical algorithm employed. The simulation framework of DSED will be further illustrated and explained in great detail in the near future papers.

Compared with experimental results, the relative errors of the simulated results are also listed in Table VI. The calculation formula of the relative error is shown in (15), where $\boldsymbol{x}_{\text{simulated}}$ and $\boldsymbol{x}_{\text{experimental}}$ are vectors of the same length, and $\boldsymbol{x}$ stands for module current i_{s1} or module voltage u_{s1}. Relative errors of DSED simulated results are close to those of Saber results, and smaller than those of Simulink results

$$\text{Relative Error} = \frac{\|\boldsymbol{x}_{\text{simulated}} - \boldsymbol{x}_{\text{experimental}}\|_2}{\|\boldsymbol{x}_{\text{experimental}}\|_2} \times 100\%. \quad (15)$$

For further illustrations of the simulated errors of different tools, Fig. 21(a) presents the comparisons of the total loss of the studied switching module. The calculation formula of E_{loss} is shown in (16), where E_{loss} is an increasing function of time. At each time step, the relative error of the simulated E_{loss} compared with the experimental E_{loss} is calculated according to (17) and plotted in Fig. 21(b). As can be observed, the relative errors of E_{loss} calculated with DSED and Saber simulated results are close, while the switching loss cannot be obtained from Simulink results

$$E_{\text{loss}}(t) = \int_0^t i_{s1} \cdot u_{s1} \cdot dt \quad (16)$$

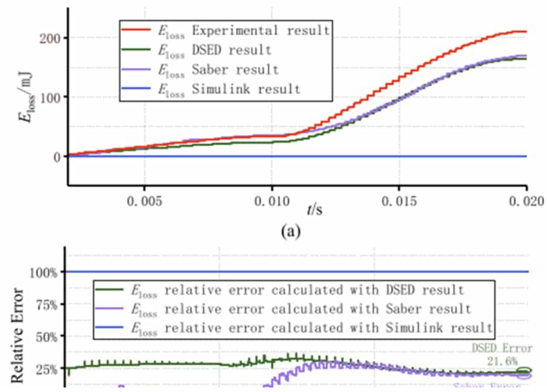
$$\text{Relative Error}(t) = \frac{|E_{\text{loss simulated}}(t) - E_{\text{loss experimental}}(t)|}{E_{\text{loss experimental}}(t)}. \quad (17)$$

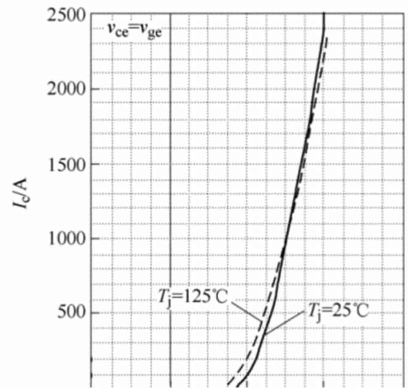
V. Conclusion

This paper proposes and demonstrates a PAT model for switching device commutation units in power electronic systems, taking an IGBT–p-i-n diode commutation unit as an ex-

TABLE VI
EXECUTION TIME COMPARISONS OF THE STUDIED DC–AC INVERTER CASE FOR SIMULATING 0.2 s

Tool	Model	Solver	Step Size	Execution Time	Relative Error (%) i_{s1}	Relative Error (%) u_{s1}
Saber	*igbt_b* and *dp1*	Gear's BDF and Newton-Raphson iteration (variable-step)	5ns with maximum step size 50ns	127s	15.83%	13.20%
Simulink	Ideal model	ode23tb (variable-step)	100ns with maximum step size 1ms	5.6s	23.32%	17.03%
DSED	PAT model	DSED method (variable-step)	Discrete state event driven with transient step size 1ns	3.5s	16.65%	14.18%





(b)

Fig. 21. (a) Total loss of the switching module calculated with the experimental and simulated results. (b) Relative errors of the total loss calculated with the simulated results compared with that calculated with the experimental results.

The manipulated figure corresponding to the altered data

combination to represent IGBT–p-i-n diode pair. According to different transient stages, it has CVS mode and VCS mode. The proposed approach ensures a reduced-order model. Comparisons confirm that PAT model is of sufficient accuracy with fast solving speed, whose parameters can be directly extracted from device datasheet. Transient models in Saber encounter the obstacle of convergence in complicated power electronic converters with numerous devices, while DSED with PAT model can easily converge with high calculation speed. Such improvements originate from the reduced-order PAT model, the event-driven simulation mechanism, and the quantization of state variables.

Further work will focus on establishing a combined electrothermal model. With thermal modeling techniques such as those demonstrated in [20]–[23], the PAT model would provide more accurate results. Besides, to ensure practicability and avoid additional experiments, complicated physical modeling approaches are abandoned in some stages in switching transients, such as the current fall stage which is modeled with

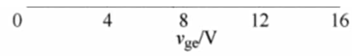


Fig. 22. Transfer characteristics given by Mitsubishi IGBT datasheet.

behavioral fitting. This generates a comparatively large error when the load current is small. Another example is the reverse recovery current I_{rr}, which is considered dominated by load current only. In fact, I_{rr} depends mostly on load current, but also on the IGBT current rise rate di_c/dt before reverse recovery. Further work will be conducted to improve the modeling accuracy. In addition, the proposed PAT modeling can be adopted to build transient models for other devices, such as silicon carbide (SiC) MOSFET and gallium nitride high electron mobility transistor (GaN HEMT). With much faster switching transients, more precise modeling of the stray parameters has to be considered. Further work will focus on adopting the more precise stray parameter model, for better description of the SiC and GaN switching transients, meanwhile improving the simulation efficiency.

Utilizing PAT model and DSED framework, large time-scale system-level dynamics and small time-scale device-level switching transients can be simulated simultaneously with high precision and efficiency. This is expected to improve the analysis, design, and control of power electronic systems.

Appendix A
Parameter Extraction of PAT Model

The device performance curves selected from manufacture datasheet [19] are presented in Figs. 22–24.

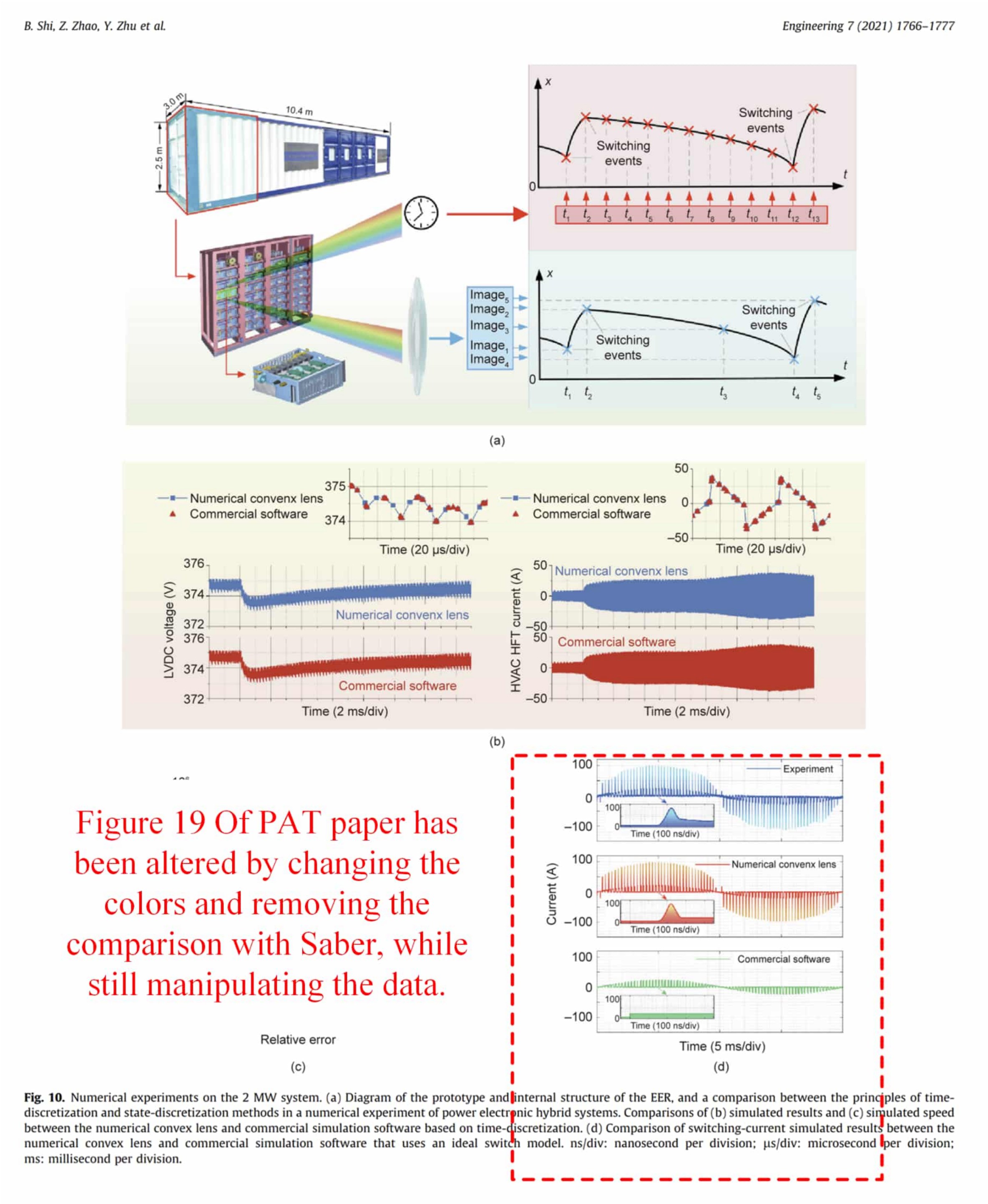


Fig. 10. Numerical experiments on the 2 MW system. (a) Diagram of the prototype and internal structure of the EER, and a comparison between the principles of time-discretization and state-discretization methods in a numerical experiment of power electronic hybrid systems. Comparisons of (b) simulated results and (c) simulated speed between the numerical convex lens and commercial simulation software based on time-discretization. (d) Comparison of switching-current simulated results between the numerical convex lens and commercial simulation software that uses an ideal switch model. ns/div: nanosecond per division; μs/div: microsecond per division; ms: millisecond per division.

02 SVID algorithm article (Top journal TIE)

This article is my second representative work. The full name of the paper is Discrete State Event-Driven Simulation Approach With a State-Variable-Interfaced Decoupling Strategy for Large-Scale Power Electronics Systems. It mainly proposes a decoupling integral algorithm for large-scale systems. The full text of the paper can be obtained by clicking link.

Problem overview

In order to highlight the characteristics of being able to simulate large-scale systems, I chose megawatt power electronic transformers developed by others in the laboratory as the research object and used their experimental waveforms. However, during the simulation, I encountered the problem that the simulation results did not match the experimental results. If I directly compared the simulation results and the experimental results on the paper, the significant difference would cause the reviewers to reject my article immediately. Therefore, I developed a method to simultaneously perform operations such as panning, zooming in, and zooming out on the vertical axis, which is the simulation data axis, and the horizontal axis, which is the simulation time axis, so that the modified simulation results and experimental results can be highly consistent.

Below I will use Fig.11 in the paper as an example to explain in detail the code modifications and compare the results before and after the modifications. The detailed data processing code and verification process can be found in [Code_for_SVID].

	Draw Code used in Paper	Code with unaltered data

Test1Plot.m

Draw Code used in Paper

```
close all
load('Test1SimandExp.mat');
load('Test2SimandExp_1.mat');
load('Test2SimandExp_2.mat');
load('Test3SimandExp.mat');
%DSED.t.1=EXP.t.1.338

index=find(ia(:,1)>0.5,1);
index2=find(ia(:,1)>1.5,1);
DSED_ia=ia(index:index2,:);
DSED_ia(:,1)=DSED_ia(:,1)-0.5;
DSED_ia(:,2)=DSED_ia(:,2)*75/70;

index=find(ib(:,1)>0.5,1);
index2=find(ib(:,1)>1.5,1);
DSED_ib=ib(index:index2,:);
DSED_ib(:,1)=DSED_ib(:,1)-0.5;
DSED_ib(:,2)=DSED_ib(:,2)*75/70;

index=find(ic(:,1)>0.5,1);
index2=find(ic(:,1)>1.5,1);
DSED_ic=ic(index:index2,:);
DSED_ic(:,1)=DSED_ic(:,1)-0.5;
DSED_ic(:,2)=DSED_ic(:,2)*75/70;

index=find(Test1_t>0.829,1);
index2=find(Test1_t>1.829,1);
EXP_t=Test1_t(index:index2)-0.829;
EXP_Current=Test1_HVACPhaseCurrent(index:index2,:);
EXP_Voltage=Test1_HVACPhaseVoltage(index:index2,:);

figure(1)
subplot(2,1,1);
plot(EXP_t,EXP_Current);

subplot(2,1,2);
plot(DSED_ib(:,1),DSED_ib(:,2));  hold on;
plot(DSED_ia(:,1),DSED_ia(:,2));  hold on;
plot(DSED_ic(:,1),DSED_ic(:,2));  hold on;
xlim([0, 1]);

figure(2)
subplot(2,1,1);
plot(EXP_t,EXP_Current); xlim([0.4,0.6]);
subplot(2,1,2);
plot(DSED_ib(:,1),DSED_ib(:,2));  xlim([0.4,0.6]);hold on;
plot(DSED_ia(:,1),DSED_ia(:,2));  xlim([0.4,0.6]);hold on;
plot(DSED_ic(:,1),DSED_ic(:,2)); xlim([0.4,0.6]);hold on;


%% Voltage
index1=find(EXP_t>0.45,1);
index2=find(EXP_t>0.55,1);
EXP_t_v=EXP_t(index1:index2);
EXP_v_045055=EXP_Voltage(index1:index2,:);

index1=find(DSED_ia(:,1)>0.45,1);
index2=find(DSED_ia(:,1)>0.55,1);

DSED_t_v=DSED_ia(index1:index2,1);
DSED_v=8165*cos(2*pi*50*DSED_t_v+pi/1.9);
DSED_v(:,2)=8165*cos(2*pi*50*DSED_t_v-2*pi/3+pi/1.9);
DSED_v(:,3)=8165*cos(2*pi*50*DSED_t_v-4*pi/3+pi/1.9);
figure();
subplot(2,1,1);
plot(EXP_t_v,EXP_v_045055);
subplot(2,1,2);
plot(DSED_t_v,DSED_v);
```

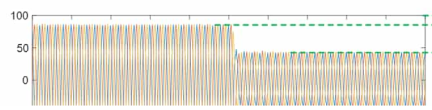
Zoom in on the simulation results

Replace the simulation results directly with the cosine function

Code with unaltered data

```
close all
load('Test1SimandExp.mat');
load('Test2SimandExp_1.mat');
load('Test2SimandExp_2.mat');
load('Test3SimandExp.mat');
%DSED.t.1=EXP.t.1.338

index=find(ia(:,1)>0.5,1);
index2=find(ia(:,1)>1.5,1);
DSED_ia=ia(index:index2,:);
DSED_ia(:,1)=DSED_ia(:,1)-0.5;
DSED_ia(:,2)=DSED_ia(:,2);

index=find(ib(:,1)>0.5,1);
index2=find(ib(:,1)>1.5,1);
DSED_ib=ib(index:index2,:);
DSED_ib(:,1)=DSED_ib(:,1)-0.5;
DSED_ib(:,2)=DSED_ib(:,2);

index=find(ic(:,1)>0.5,1);
index2=find(ic(:,1)>1.5,1);
DSED_ic=ic(index:index2,:);
DSED_ic(:,1)=DSED_ic(:,1)-0.5;
DSED_ic(:,2)=DSED_ic(:,2);

index=find(Test1_t>0.829,1);
index2=find(Test1_t>1.829,1);
EXP_t=Test1_t(index:index2)-0.829;
EXP_Current=Test1_HVACPhaseCurrent(index:index2,:);
EXP_Voltage=Test1_HVACPhaseVoltage(index:index2,:);

figure(1)
subplot(2,1,1);
plot(EXP_t,EXP_Current);

subplot(2,1,2);
plot(DSED_ib(:,1),DSED_ib(:,2));  hold on;
plot(DSED_ia(:,1),DSED_ia(:,2));  hold on;
plot(DSED_ic(:,1),DSED_ic(:,2));  hold on;
xlim([0, 1]);

figure(2)
subplot(2,1,1);
plot(EXP_t,EXP_Current); xlim([0.4,0.6]);
subplot(2,1,2);
plot(DSED_ib(:,1),DSED_ib(:,2));  xlim([0.4,0.6]);hold on;
plot(DSED_ia(:,1),DSED_ia(:,2));  xlim([0.4,0.6]);hold on;
plot(DSED_ic(:,1),DSED_ic(:,2)); xlim([0.4,0.6]);hold on;


%% Voltage
index1=find(EXP_t>0.45,1);
index2=find(EXP_t>0.55,1);
EXP_t_v=EXP_t(index1:index2);
EXP_v_045055=EXP_Voltage(index1:index2,:);

index1=find(DSED_ia(:,1)>0.45,1);
index2=find(DSED_ia(:,1)>0.55,1);

DSED_t_v=DSED_ia(index1:index2,1);
DSED_v=8165*cos(2*pi*50*DSED_t_v+pi/1.9);
DSED_v(:,2)=8165*cos(2*pi*50*DSED_t_v-2*pi/3+pi/1.9);
DSED_v(:,3)=8165*cos(2*pi*50*DSED_t_v-4*pi/3+pi/1.9);
figure();
subplot(2,1,1);
plot(EXP_t_v,EXP_v_045055);
subplot(2,1,2);
plot(DSED_t_v,DSED_v);
```

Replace the simulation results directly with the cosine function



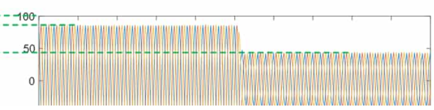


Fig.A1

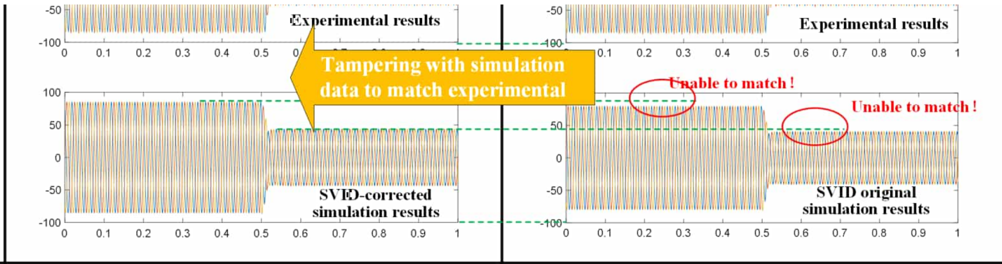


Fig.A2

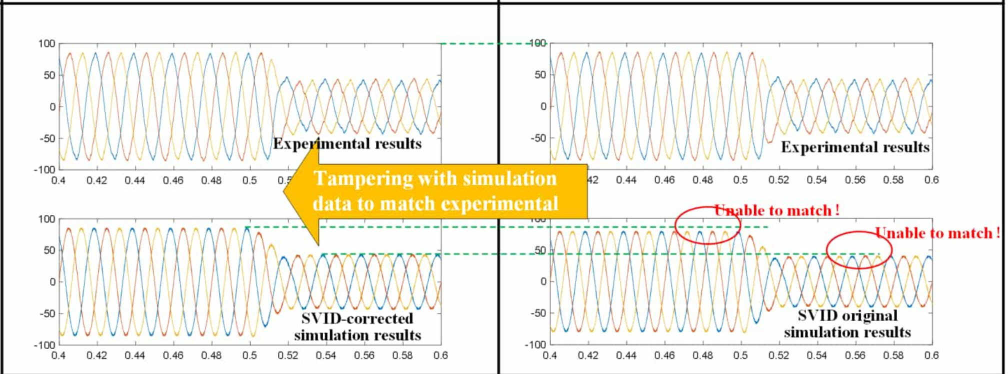
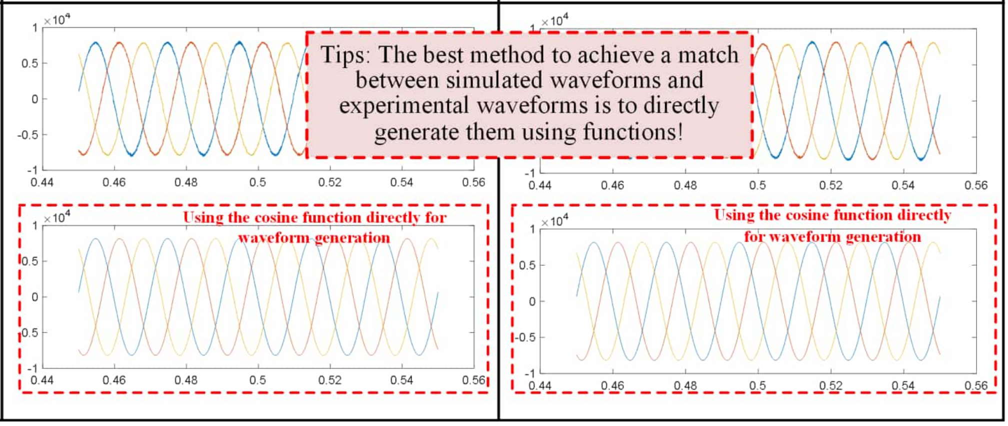


Fig.A3



	Draw Code used in Paper	Code with unaltered data

Test2Plot.m

Draw Code used in Paper (tabs: Test1Plot.m, Test2Plot.m *, Test3Plot.m)

```
close all;

Test2_uBUS_1_sim_mod=(Test2_uBUS_1_sim-675)*10+680;
Test2_DSED_i=(Test2_i_1_sim+1095)*0.9-1095;
Test2_DSED_ti=Test2_t_2_si        3+0.015;
index1=find(Test2_DSED_ti>0,
index2=find(Test2_DSED_ti>0.0
Test2_DSED_i=Test2_DSED_i(index1
Test2_DSED_v=Test2_uBUS_1_sim_mo
Test2_DSED_ti=Test2_DSED_ti(index1:index2);
index3=find(Test2_DSED_ti>0.012,1);
Test2_DSED_ti(index3:end)=(Test2_DSED_ti(index3:end)
    -0.012)*1.5+0.012;


index1=find(Test2_t>3.11,1)
index2=find(Test2_t>3.16,1);
Test2_EXP_t=Test2_t(index1:inde
Test2_EXP_i=Test2_DCCurrent(index1:index
Test2_EXP_Bus=Test2_LVDCCurrent(index1:index2);

figure();
subplot(2,1,1);
plot(Test2_EXP_t,Test2_EXP_i);
xlim([0, 0.05]);
subplot(2,1,2);
plot(Test2_DSED_ti,Test2_DSED_i);
xlim([0, 0.05]);
figure();
subplot(2,1,1)
plot(Test2_EXP_t,Test2_EXP_Bus);
xlim([0, 0.05]);
subplot(2,1,2)
plot(Test2_DSED_ti,Test2_DSED_v);
xlim([0, 0.05]);
```

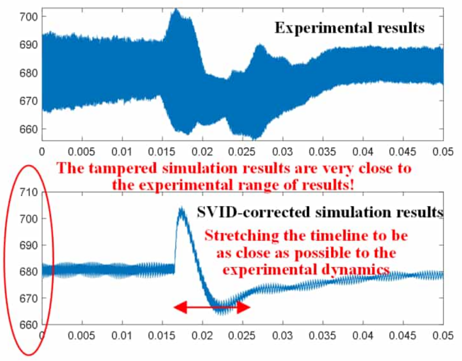
Code with unaltered data (tabs: Test1Plot.m, Test2Plot.m, Test3Plot.m)

```
close all;

Test2_uBUS_1_sim_mod=(Test2_uBUS_1_sim);
Test2_DSED_i=(Test2_i_1_sim);
Test2_DSED_ti=Test2_t     sim-0.3+0.015;
                    0,1);
                    i>0.05,1);
                    D_i(index1:index2);
                    _uBUS_1_sim_mod(index1:index2);
Test2_DSED_ti=Test2_DSED_ti(index1:index2);
index3=find(Test2_DSED_ti>0.012,1);
Test2_DSED_ti(index3:end)=(Test2_DSED_ti(index3:end));


                    1,1);
                    16,1);
                    t(index1:index2)-3.11;
Test2_EXP_i=Test2_DCCurrent(index1:index2);
Test2_EXP_Bus=Test2_LVDCCurrent(index1:index2);

figure();
subplot(2,1,1);
plot(Test2_EXP_t,Test2_EXP_i);
xlim([0, 0.05]);
subplot(2,1,2);
plot(Test2_DSED_ti,Test2_DSED_i);
xlim([0, 0.05]);
figure();
subplot(2,1,1)
plot(Test2_EXP_t,Test2_EXP_Bus);
xlim([0, 0.05]);
subplot(2,1,2)
plot(Test2_DSED_ti,Test2_DSED_v);
xlim([0, 0.05]);
```

To fit the experimental results, one approach is to adjust the simulated results by scaling and vertically shifting them.

To fit the dynamic behavior, you can try adjusting the simulation results by scaling and horizontally shifting the time axis.

Fig.A4



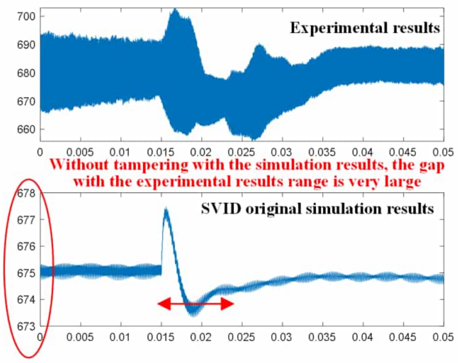
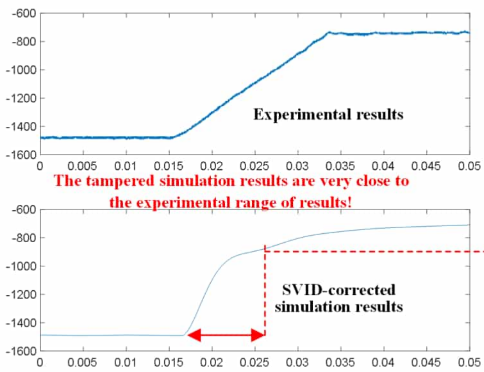
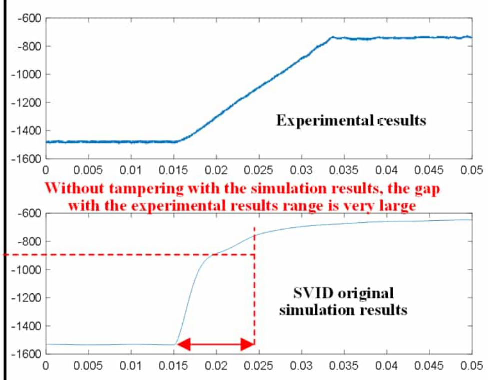
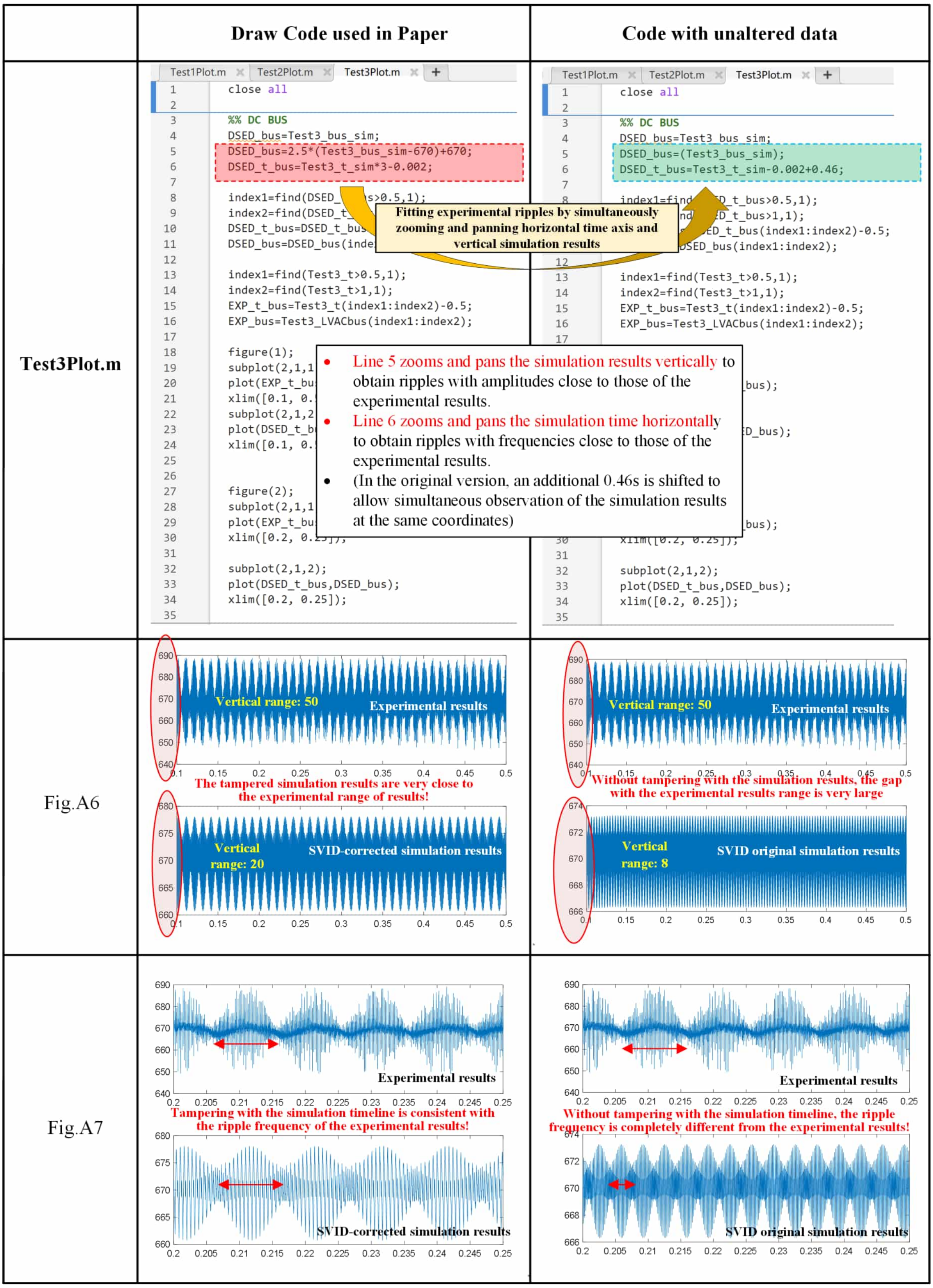


Fig.A5







Solution effect

Through the above efforts, I completely solved the underlying problem of the inconsistency between SVID simulation results and experimental results. Furthermore, the processed data in matlab were plotted using professional drawing software, where Fig.A1-A2 and Fig.A6-A7 are shown in Fig11 of journal article, and Fig.A1-A7 is shown in my doctoral thesis.

SHI *et al.*: DSED SIMULATION APPROACH WITH A SVID STRATEGY FOR LARGE-SCALE POWER ELECTRONICS SYSTEMS 11681

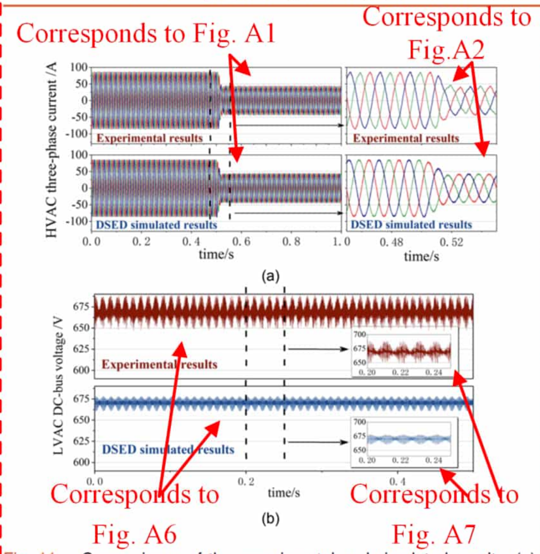


Fig. 11. Comparisons of the experimental and simulated results. (a) Grid-side current of the HVac port under the sudden change of the power command [31]. (b) DC bus voltage of the LVac port in the steady state.

Tampering with experimental and simulation data! !

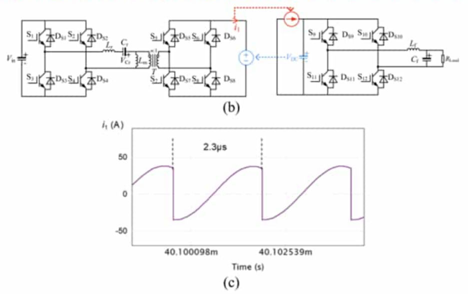


Fig. 12. Studied smaller cases. (a) Two-stage case. (b) Decoupled system. (c) Simulated results of the interfaced current i_1.

the inverter stay in the same subsystem. With such a partitioning way, the dynamics of the dc-link capacitor is relatively slow (the dc voltage changes around 400 V), and therefore, it seems that even with some delay/latency of the interface variables, the difference in simulation accuracy may not be observable. However, one significant fact that must be considered is that the dynamics of the interfaced current is fast. It exhibits switching behavior, as shown in Fig. 12(c). Besides, during two switching events, it varies rapidly in a resonant manner. Therefore, with the conventional decoupling method that introduces "one-step delay," the accuracy will be largely damaged. To prove this,

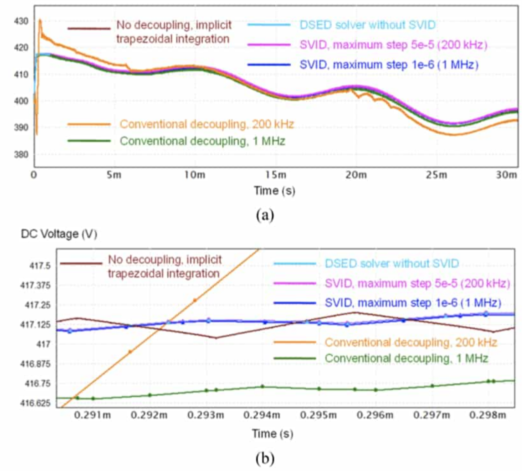


Fig. 13. Comparisons of the SVID method with other decoupling methods. The simulated results of the dc-link voltage (V_{DC} in Fig. 12) are presented. (a) 30 ms view. (b) Zoomed-in view.

Fig. 13(a) provides the comparisons of the accurate results (DSED solver without decoupling) with the conventional decoupling method, which uses the previous step value in the current step. With a 200 kHz rate (e.g., 5 μs delay), the results of the dc voltage are significantly different. Even with a 1 MHz rate (e.g., 1 μs delay), the difference is still observable. As for the SVID method, it gives highly accurate results compared with both DSED results (without decoupling) and with simulated results from other implicit solvers (trapezoidal integration).

F. Generalization of the Method

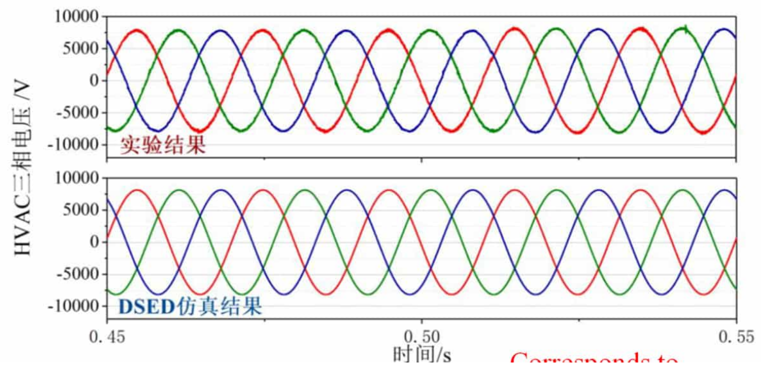
The proposed SVID method is a general method for the arbitrary power electronics circuit. The automatic partitioning of the circuit can be conducted with the following algorithm.

1) Find all the capacitors in the circuit.
2) Remove each capacitor.
3) Test the connectedness of the new graph with the depth-first-search method [32].
4) Identify the subsystems and repeat the above-mentioned procedures.

The statement that the SVID method does not sacrifices accuracy compared with the FA-DS algorithm [15] without decoupling can be proved with the substitution theorem [33]: "In an arbitrary network, any uncoupled branch may be replaced either by an independent voltage source or by an independent current source with the same voltage or current waveform, respectively, as the branch, without affecting the branch voltages, currents, or waveforms in the remainder of the network." With this theorem, it can be proved that the LTE of each step in FA-DS is the same with or without the SVID method presented in this article.

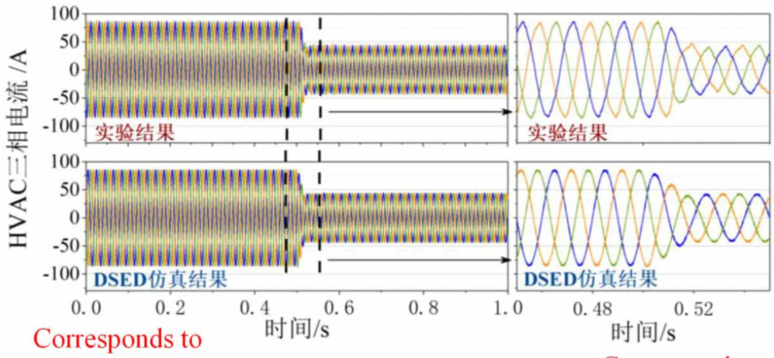
The mathematical justifications of the efficiency of the SVID method can be provided by comparing the number of calculations in the integration algorithm [34] with and without the

第 4 章　电力电子混杂系统解耦型仿真方法



Corresponds to
Fig. A3

(a) 三相电压



Corresponds to
Fig. A1

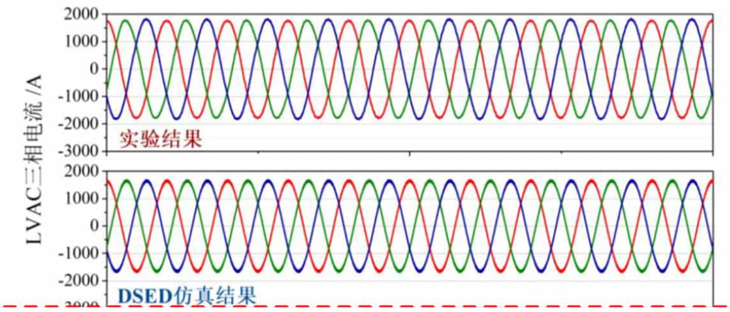
(b) 三相电流

Corresponds to
Fig. A2

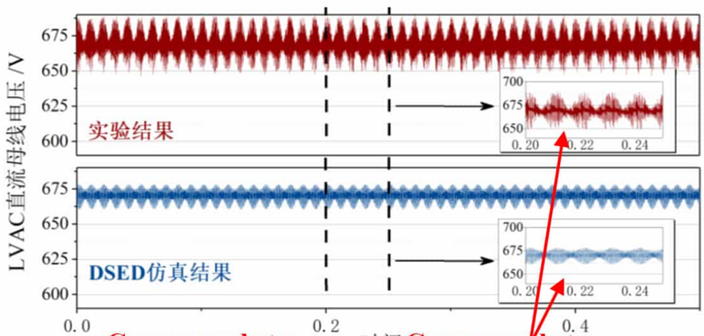
图4.16 HVAC实验结果对比

Tampering with experimental and simulation data! !

104

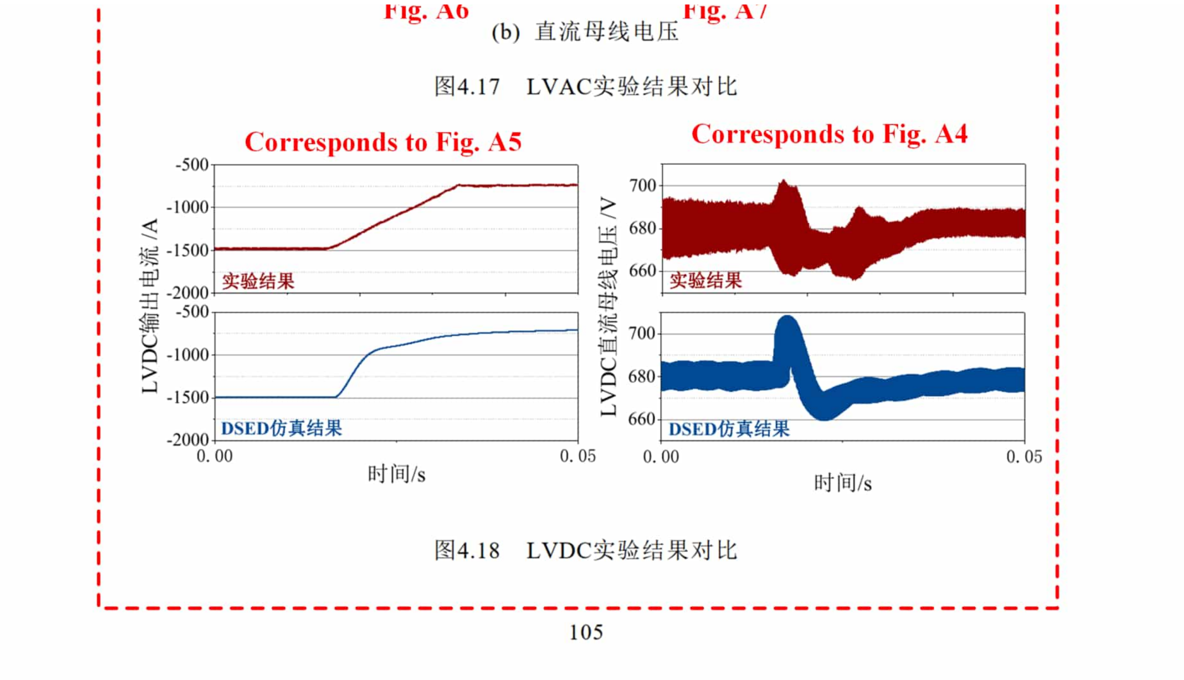


Tampering with experimental and simulation data! !



Corresponds to

Corresponds to



Eff Application Article (Top Journal TIE)

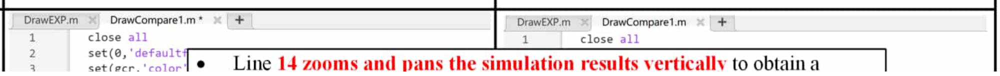
This article is my third representative work. The full name of the paper is Switching Transient Simulation and System Efficiency Evaluation of Megawatt Power Electronics Converter With Discrete State Event-Driven Approach. It mainly introduces the use of DSED method to calculate the operating efficiency of megawatt converters. The full text of the paper can be obtained by clicking link.

Problem overview

In order to be able to calculate the losses of a megawatt converter, I first need to prove in the paper that my simulation results are consistent with the experimental results, so I need to compare the simulated waveform with the actual waveform, as shown in Fig.15 in the paper. However, during the simulation, I encountered the problem that the simulation results did not match the experimental results. If I directly compared the simulation results and the experimental results on the paper, the significant difference would cause the reviewers to reject my article immediately. Therefore, I developed the ability to simultaneously pan, zoom in, and zoom out on the vertical axis, which is the simulation data axis, and the horizontal axis, which is the simulation time axis. In addition, I also added a new method of directly using mathematical functions to fabricate simulation results. , so that the modified simulation results and experimental results can be highly consistent.

Below I will use Fig.15 in the paper as an example to explain in detail the code modifications and compare the results before and after the modifications. The detailed data processing code and verification process can be found in Code_for_Eff.

	Draw Code used in Paper	Code with unaltered data



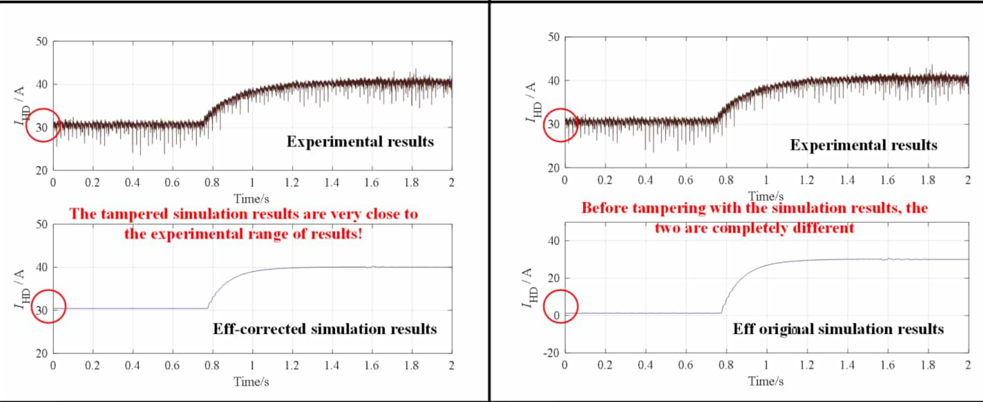
DrawCompare1 Code snippet1

```
4
5   figure(1);
6   subplot(2,1,1);
7   plot(Test1IHVDC
8   xlim([0,2]); yl
9   ylabel("\itI\rm
10  set(gca,'FontNa
11  set(gca,'FontSi
12
13  DSIMIHVDC=csvread("DSIM-IHVDC.csv",1,0);
14  DSIMIHVDC(:,2)=(DSIMIHVDC(:,2))/3+30;
15  DSIMIHVDC(:,1)=(DSIMIHVDC(:,1)-DSIMIHVDC(1,1)-0.04)/0.6*10;
16  subplot(2,1,2);
17  plot(DSIMIHVDC(:,1),DSIMIHVDC(:,2),'color','#3b2e7e');
18  xlim([0,2]);  ylim([20,50]); xlabel("Time/s");
19  ylabel("\itI\rm_H_D / A"); grid on;
20  set(gca,'FontName','Times New Roman');
21  set(gca,'FontSize',10);
```

- dynamic range **close** to the experimental results
- Line **15 zooms and pans the simulation time horizontally** to obtain a dynamic range **close** to the experimental results.
- (The code in the original version is retained because the modification time is difficult to compare)

```
    ','#4c221b');
12
13  DSIMIHVDC=csvread("DSIM-IHVDC.csv",1,0);
14  DSIMIHVDC(:,2)=(DSIMIHVDC(:,2));
15  DSIMIHVDC(:,1)=(DSIMIHVDC(:,1)-DSIMIHVDC(1,1)-0.04)/0.6*10;
16  subplot(2,1,2);
17  plot(DSIMIHVDC(:,1),DSIMIHVDC(:,2),'color','#3b2e7e');
18  xlim([0,2]);  ylim([-20,50]); xlabel("Time/s");
19  ylabel("\itI\rm_H_D / A"); grid on;
20  set(gca,'FontName','Times New Roman');
21  set(gca,'FontSize',10);
```

Fig. B1



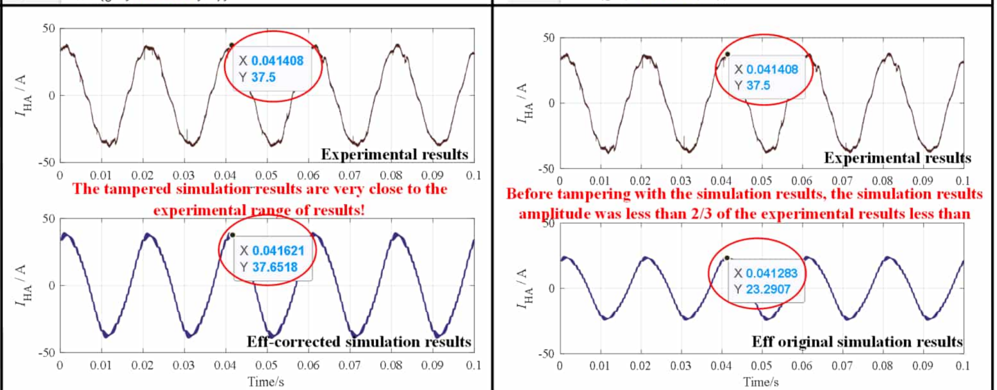
DrawCompare1 Code snippet2

```
23  figure(2);
24  subplot(2,1,1);
25  plot(Test2IC1(:,1),Test2IC1(:,2),'color','#4c221b');
26  xlim([0,0.1
27  ylim([-50,5
28  xlabel("Tim
29  ylabel("\it
30  set(gca,'Fo
31  set(gca,'FontSize',10);
32
33  DSIMIHVDC=csvread("DSIM-IC1.csv",1,0);
34  DSIMIHVDC(:,2)=(DSIMIHVDC(:,2))/23*37;
35  DSIMIHVDC(:,1)=DSIMIHVDC(:,1)-0.6732;
36  subplot(2,1,2);
37  plot(DSIMIHVDC(:,1),DSIMIHVDC(:,2),'color','#3b2e7e');
38  xlim([0,0.1]);
39  ylim([-50,50]);
40  xlabel("Time/s");
41  ylabel("\itI\rm_H_A / A"); grid on;
42  set(gca,'FontName','Times New Roman');
43  set(gca,'FontSize',10);
```

- Line **34 amplifies** the simulation results by **a factor of 37/23 (1.6)** to obtain an amplitude close to the experimental results

```
23  figure(2);
24  subplot(2,1,1);
25  plot(Test2IC1(:,1),Test2IC1(:,2),'color','#4c221b');
31  set(gca,'FontSize',10);
32
33  DSIMIHVDC=csvread("DSIM-IC1.csv",1,0);
34  DSIMIHVDC(:,2)=(DSIMIHVDC(:,2));
35  DSIMIHVDC(:,1)=DSIMIHVDC(:,1)-0.6732;
36  subplot(2,1,2);
37  plot(DSIMIHVDC(:,1),DSIMIHVDC(:,2),'color','#3b2e7e');
38  xlim([0,0.1]);
39  ylim([-50,50]);
40  xlabel("Time/s");
41  ylabel("\itI\rm_H_A / A"); grid on;
42  set(gca,'FontName','Times New Roman');
43  set(gca,'FontSize',10);
```

Fig. B2



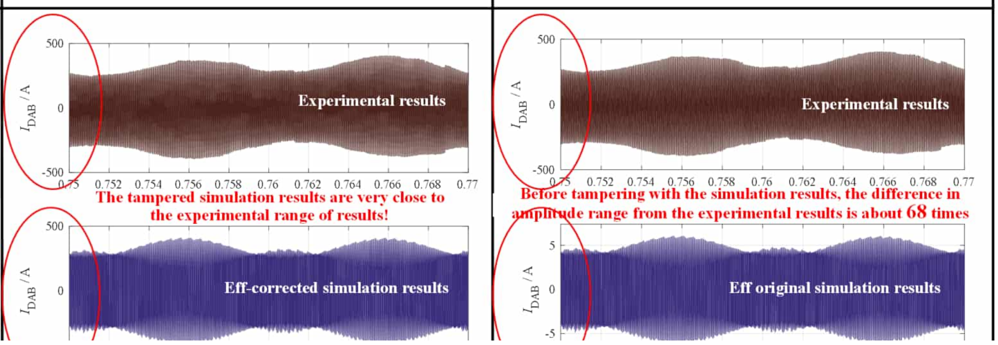
DrawCompare1 代码片段3

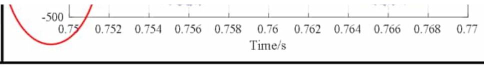
```
47  figure(3);
48  subplot(2,1,1);
49  plot(Test2IHVAC1(:,1),Test2IHVAC1(:,2),'color','#4c221b');
50  xlim([0.75,0.77]);
51  ylim([-500,500
52  xlabel("Time/s
53  ylabel("\itI\r
54  set(gca,'FontN
55  set(gca,'FontSize',10);
56
57  DSIMIHVAC2=csvread("DSIM-IHVAC2.csv",1,0);
58  DSIMIHVAC2(:,2)=(DSIMIHVAC2(:,2))/6*405;
59  DSIMIHVAC2(:,1)=DSIMIHVAC2(:,1)-0.1616+0.75;
60  subplot(2,1,2);
61  plot(DSIMIHVAC2(:,1),DSIMIHVAC2(:,2),'color','#3b2e7e');
62  xlim([0.75,0.77]);
63  ylim([-500,500]);
64  xlabel("Time/s");
65  ylabel("\itI\rm_D_A_B / A"); grid on;
66  set(gca,'FontName','Times New Roman');
67  set(gca,'FontSize',10);
```

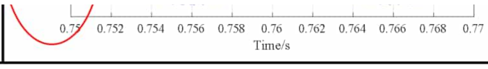
- Line **58 amplifies** the simulation results by **a factor of 405/6 (67.5)** to obtain an amplitude close to the experimental results

```
47  figure(3);
48  subplot(2,1,1);
49  plot(Test2IHVAC1(:,1),Test2IHVAC1(:,2),'color','#4c221b');
50  xlim([0.75,0.77]);
55  set(gca,'FontSize',10);
56
57  DSIMIHVAC2=csvread("DSIM-IHVAC2.csv",1,0);
58  DSIMIHVAC2(:,2)=(DSIMIHVAC2(:,2));
59  DSIMIHVAC2(:,1)=DSIMIHVAC2(:,1)-0.1616+0.75;
60  subplot(2,1,2);
61  plot(DSIMIHVAC2(:,1),DSIMIHVAC2(:,2),'color','#3b2e7e');
62  xlim([0.75,0.77]);
63  ylim([-500*6/405,500*6/405]);
64  xlabel("Time/s");
65  ylabel("\itI\rm_D_A_B / A"); grid on;
66  set(gca,'FontName','Times New Roman');
67  set(gca,'FontSize',10);
```

Fig. B3







	Draw Code used in Paper	Code with unaltered data

DrawCompare1 Code snippet4

Draw Code used in Paper:

```
70  figure(4);
71  subplot(2,1,1);
72  plot(Test2IHVAC1(:,1),Test2IHVAC1(:,2),'color','#4c221b');
73  xlim([0.75
74  ylim([-500
75  xlabel("Ti
76  ylabel("\i
77  set(gca,'F
78  set(gca,'FontSize',10);
79
80  subplot(2,1,2);
81  DSIMIHVAC2(:,2)= DSIMIHVAC2(:,2)*345/401
82  plot(DSIMIHVAC2(:,1),DSIMIHVAC2(:,2),'color','#3b2e7e');
83  xlim([0.755,0.755+0.0005]);
84  ylim([-500,500]);
85  xlabel("Time/s");
86  ylabel("\itI\rm_D_A_B / A"); grid on;
87  set(gca,'FontName','Times New Roman');
88  set(gca,'FontSize',10);
```

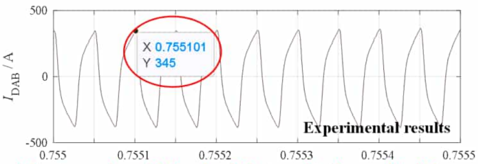
- Line **81** is further fine-tuned after code snippet 3 is **scaled up** by **a factor of 67.5** to **reduce** the simulation result by **a factor of 345/401 (0.86)** to obtain a magnitude close to the experimental result

Code with unaltered data:

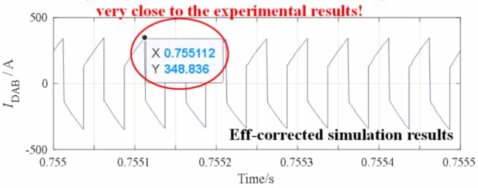
```
70  figure(4);
71  subplot(2,1,1);
72  plot(Test2IHVAC1(:,1),Test2IHVAC1(:,2),'color','#4c221b');
78  set(gca,'FontSize',10);
79
80  subplot(2,1,2);
81  DSIMIHVAC2(:,2)= DSIMIHVAC2(:,2);
82  plot(DSIMIHVAC2(:,1),DSIMIHVAC2(:,2),'color','#3b2e7e');
83  xlim([0.755,0.755+0.0005]);
84  ylim([-500*6/405/345*401,500*6/405/345*401]);
85  xlabel("Time/s");
86  ylabel("\itI\rm_D_A_B / A"); grid on;
87  set(gca,'FontName','Times New Roman');
88  set(gca,'FontSize',10);
```

Fig. B4

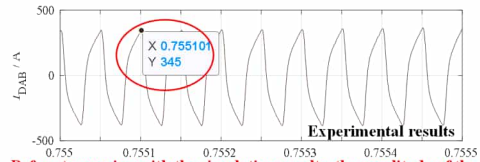
Draw Code used in Paper:



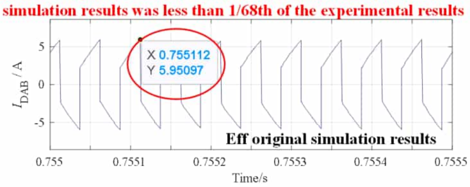
After tampering with the simulation results, the amplitude is very close to the experimental results!



Code with unaltered data:



Before tampering with the simulation results, the amplitude of the simulation results was less than 1/68th of the experimental results



DrawCompare1 Code snippet5

Draw Code used in Paper:

```
92  figure(5);
93  subplot(2,1,1);
94  plot(Test2YBLVDC(:,1),Test2YBLVDC(:,2),'color','#4c221b');
95  xlim([0.03211,0.03211+0.00025]);
96  ylim(
97  xlabe
98  ylabe
99  set(g
100 set(gca,'FontSize',10);
101
102 DSIMYBLVDC=csvread("DSIM-YBLVDC.csv",1,0);
103 DSIMYBLVDC(:,2)=(DSIMYBLVDC(:,2))*1.01604;
104
105 DSIMYBLVDC(:,1)=DSIMYBLVDC(:,1)-0.0162874+0.03211;
106 subplot(2,1,2);
107 plot(DSIMYBLVDC(:,1),DSIMYBLVDC(:,2),'color','#3b2e7e');
108 xlim([0.03211,0.03211+0.00025]);
109 ylim([-2000,2000]);
110 xlabel("Time/s");
111 ylabel("\itU\rm_H_L_A / A"); grid on;
112 set(gca,'FontName','Times New Roman');
113 set(gca,'FontSize',10);
```

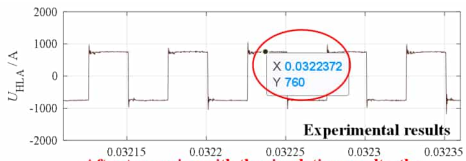
- Line **103 amplifies** the simulation results by **a factor of 1.01604** to obtain an amplitude that is essentially the same as the experimental results

Code with unaltered data:

```
92  figure(5);
93  subplot(2,1,1);
94  plot(Test2YBLVDC(:,1),Test2YBLVDC(:,2),'color','#4c221b');
95  xlim([0.03211,0.03211+0.00025]);
100 set(gca,'FontSize',10);
101
102 DSIMYBLVDC=csvread("DSIM-YBLVDC.csv",1,0);
    DSIMYBLVDC(:,2)=(DSIMYBLVDC(:,2));
104
105 DSIMYBLVDC(:,1)=DSIMYBLVDC(:,1)-0.0162874+0.03211;
106 subplot(2,1,2);
107 plot(DSIMYBLVDC(:,1),DSIMYBLVDC(:,2),'color','#3b2e7e');
108 xlim([0.03211,0.03211+0.00025]);
109 ylim([-2000,2000]);
110 xlabel("Time/s");
111 ylabel("\itU\rm_H_L_A / A"); grid on;
112 set(gca,'FontName','Times New Roman');
113 set(gca,'FontSize',10);
```

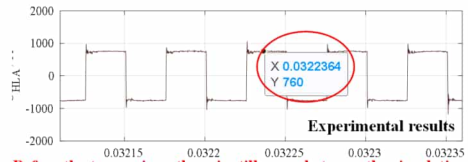
Fig. B5

Draw Code used in Paper:

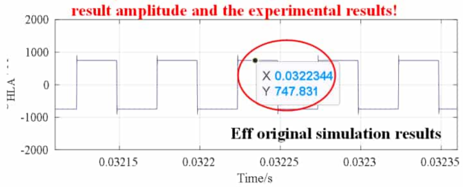


After tampering with the simulation results, the amplitude is very close to the experimental results!

Code with unaltered data:



Before the tampering , there is still a gap between the simulation result amplitude and the experimental results!



DrawCompare1 Code snippet6

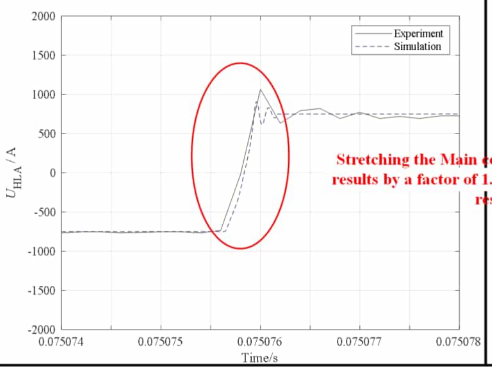
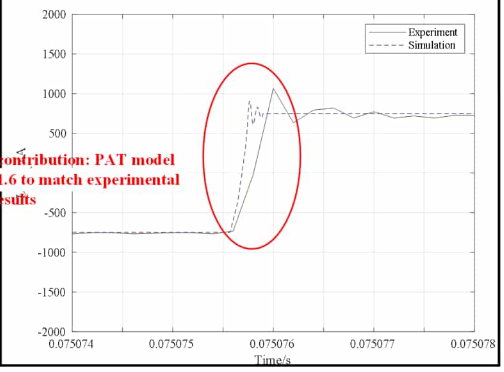
Draw Code used in Paper:

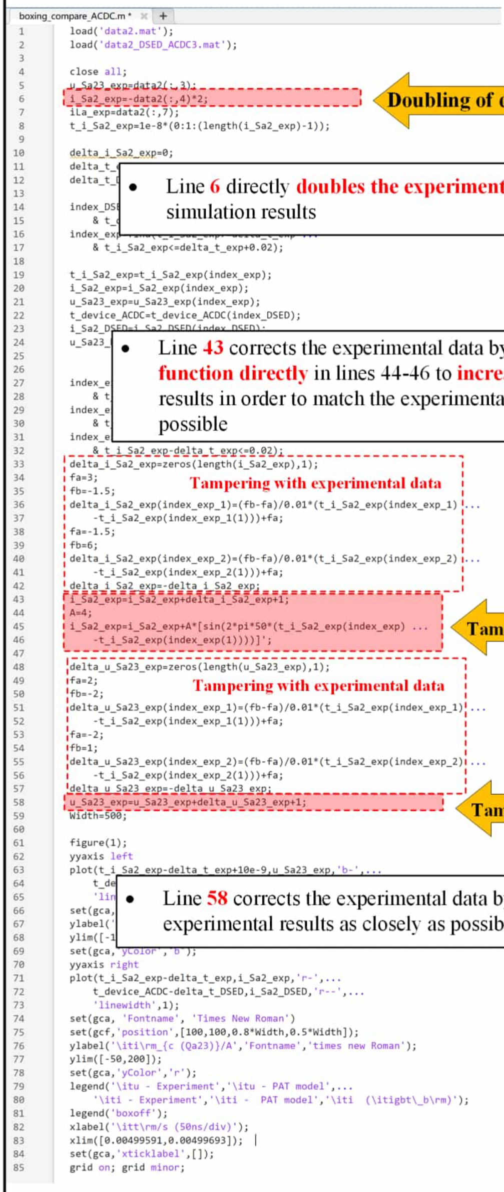
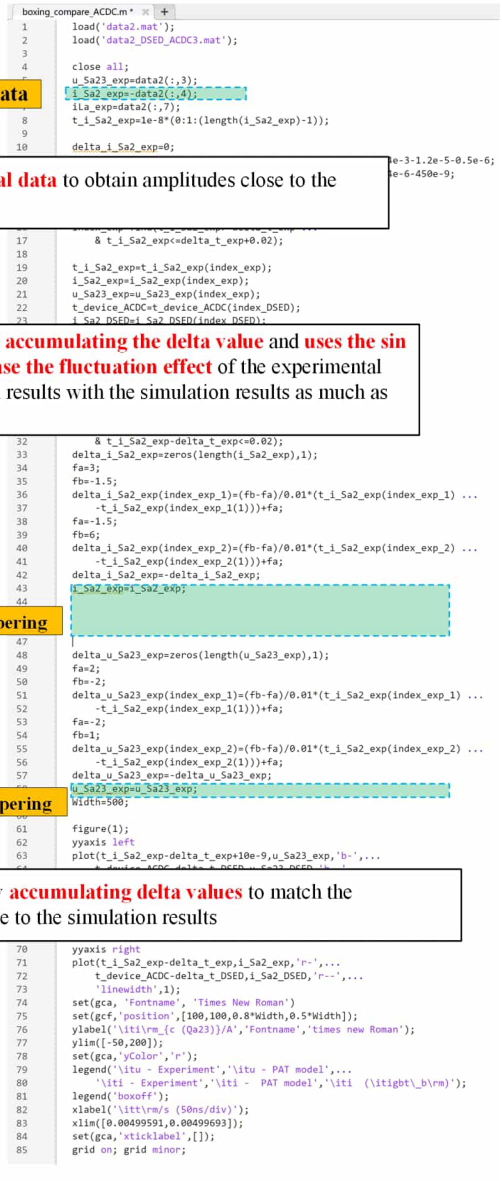
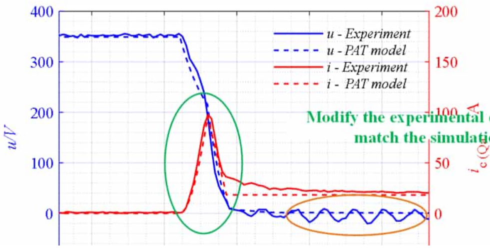
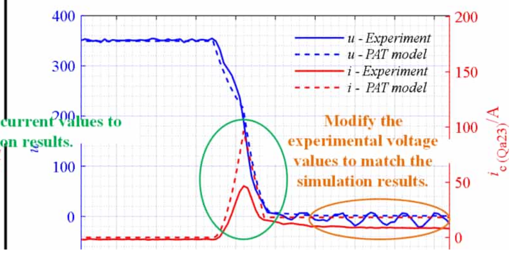
```
116 figure(6);
117 % subplot(
118 plot(Test2
119 hold on;
120 xlim([0.07
121 ylim([-200
122 xlabel("Ti
123 ylabel("\itU\rm_H_L_A / A"); grid on;
124 set(gca,'FontName','Times New Roman');
125 set(gca,'FontSize',10);
126
127 DSIMTR1=csvread("DSIM-TR-1.csv",1,0);
128 DSIMTR1(:,1)=(DSIMTR1(:,1))*1.6;
129 DSIMTR1(:,1)=(DSIMTR1(:,1))-DSIMTR1(1,1)+0.075074-0.00
130 plot(DSIMTR1(:,1),DSIMTR1(:,2),'--','color','#3b2e7e');
131 legend ('Experiment','Simulation');
132 set(gca,'FontName','Times New Roman');
133 set(gca,'FontSize',10);
```

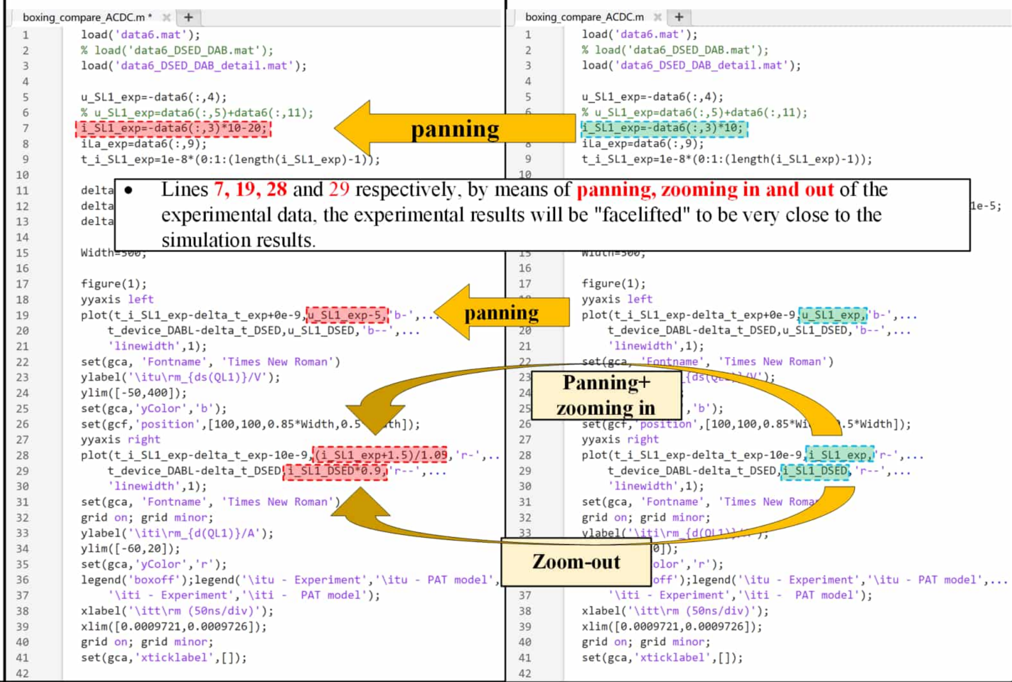
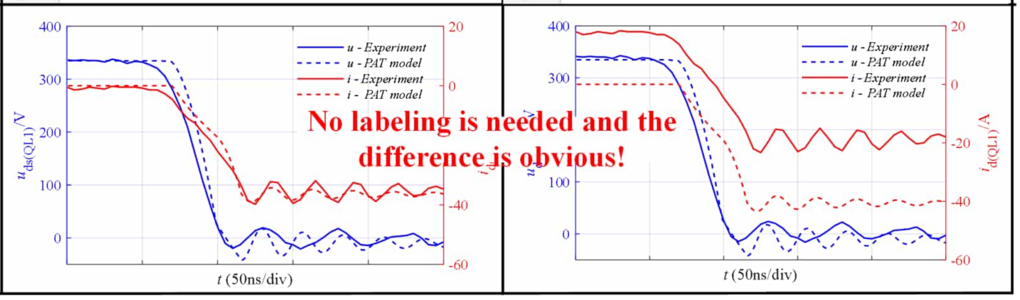
- Line **128 scales up** the simulation time by **a factor of 1.6** to obtain a dynamic time close to the experimental results
- (Line 129 adds an additional 0.0000072s to regain the same starting point of the action)

Code with unaltered data:

```
116 figure(6);
123 ylabel("\itU\rm_H_L_A / A"); grid on;
124 set(gca,'FontName','Times New Roman');
125 set(gca,'FontSize',10);
126
127 DSIMTR1=csvread("DSIM-TR-1.csv",1,0);
128 DSIMTR1(:,1)=(DSIMTR1(:,1));
129 DSIMTR1(:,1)=(DSIMTR1(:,1))-DSIMTR1(1,1)+0.075074-0.0000111*1.6+0.0000072
130 plot(DSIMTR1(:,1),DSIMTR1(:,2),'--','color','#3b2e7e');
131 legend ('Experiment','Simulation');
132 set(gca,'FontName','Times New Roman');
133 set(gca,'FontSize',10);
```

Fig. B6		

	Draw Code used in Paper	Code with unaltered data
02 Folder Code		
Fig. B7		

	
03 Folder Code	
Fig. B8	

Solution effect

Through the above efforts, I completely solved the underlying problem of the inconsistency between simulation results and experimental results in loss calculation. Furthermore, the processed data in MATLAB was plotted using professional drawing software, where Fig.B1-B8 correspond to Fig.15 (a)-(5) in journal article, and I also wrote it in my doctoral thesis.

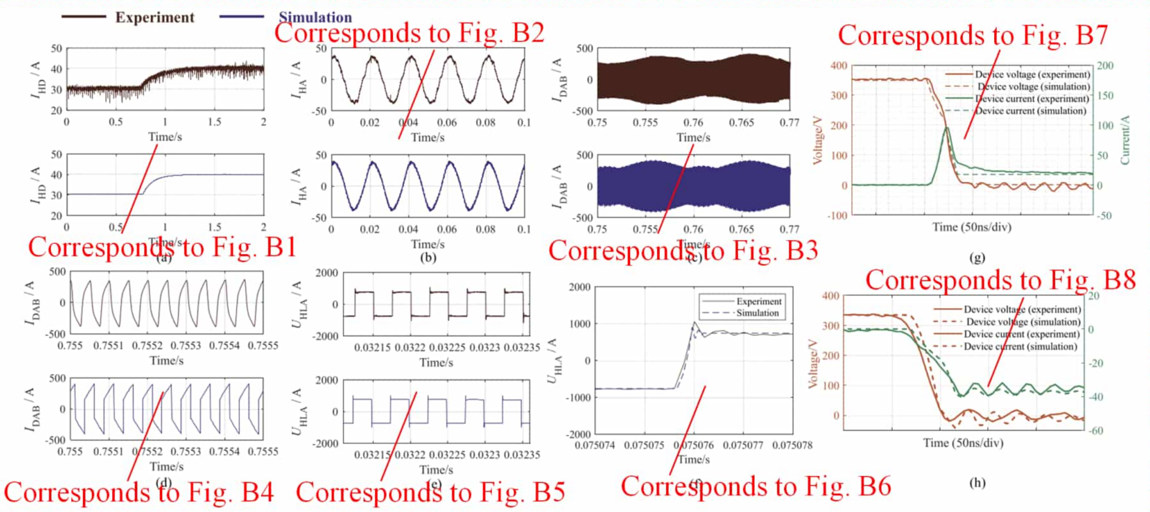


Fig. 15. Comparisons of simulated and experimental results: (a) current of 10 kV dc port; (b) current of 10 kV ac port; (c) current of 10 kV ac port HFT and (d) its zoomed-in view; (e) voltage of the output port of the H-bridge in 750 V dc port and (f) its zoomed-in view; (g) current and voltage of a turn-ON transient of the IGBT and (h) current and voltage of a turn-OFF transient of the SiC MOSFET in a 50 kVA PET.

Tampering with experimental and simulation data! !

it is hardly possible to use them in this megawatt case study composed of more than 500 switching devices and hundreds of H-bridges. The major concern is the convergence problems. Therefore, a system-level commercial tool with ideal switch model, which is more suitable for large-system design and complicated control design in practical applications, is selected. But the comparisons with this commercial software only attest to the accuracy of the proposed method in terms of system-level dynamics. The simulated results are also compared with experimental results to verify the transient results. The photograph of the experimental prototype is shown in Fig. 14. A load change of the 10-kV dc port is tested, with a step change of the power flow from 300 to 400 kW. The current of the 10-kV dc port is shown in Fig. 15(a), defined as I_{HD}, and the current of the 10-kV ac port is shown in Fig. 15(b), defined as I_{HA}. The HFT current in 10 kV ac stage, namely, the dual-active-bridge (DAB) current I_{DAB}, is shown in Fig. 15(c), and Fig. 15(d) is the zoomed-in view. Finally, the output voltage U_{HLA} of the H-bridge in the DAB in 380 V ac port is shown in Fig. 15(e), which consists of the device-level switching transients, with the zoomed-in comparison presented in Fig. 15(f). In general, the simulated results are in good agreement with the experimentally measured ones.

Fig. 15(a)–(f) only shows the transient results of the device voltage because it is very hard to measure the device current in the real prototype of a high-power converter. As a result, switching transient simulations are also performed on a smaller system: a 50-kVA PET as a smaller portion of the studied 2 MW PET [35], [42]. The 50-kVA PET consists of 16 IGBTs and eight SiC MOSFETs. The detailed structure of the 50-kVA PET can be found in [35]. The results are compared in Fig. 15(g) and (h), which also show good agreement.

V. System Efficiency Evaluation Based on the Proposed Method

With the fast simulation speed and the ability to capture switching transients, the proposed method enables the in-depth analysis of the PET. To further demonstrate the value of the proposed method in practical development and research, one representative application, namely, the evaluation of the system efficiency is studied. As an energy conversion system, ensuring high efficiency is always of essential significance. But the efficiency of the system is strongly dependent on the operational conditions. To accurately simulate the efficiency curve, the real control strategies must be implemented in the simulation, the real structure of the system must be modeled, and the switching transients which can lead to substantial switching losses must be simulated. Therefore, the proposed method offers a possibility to accurately and efficiently simulate the efficiency curve during the design stage.

Here, we first discuss the general loss distribution of a power electronics system. Generally, the input power of the converter P_{in} equals the sum of the output power P_{out} and the total loss P_{loss}. Components that contribute to P_{loss} include ON-state loss of the semiconductor switches P_{on}, switching loss of the switches P_{sw}, cooper loss of the transformers P_{Cu}, iron loss of the transformer P_{Fe}, loss of the equivalent series resistance (ESR) P_{ESR}, and the additional loss P_0. They can be classified into fixed loss P_{fixed}, which is irrelevant of the load current, switching loss P_{sw}, which is proportional to the load current, and resistive loss P_{R}, which is proportional to the square of the load current [43]. Therefore, it can be deduced that a typical efficiency curve exhibits a convex feature shown in Fig. 16. Under light load, the fixed loss P_{fixed} contributes to a big proportion in the total loss; therefore, the efficiency is low. Under heavy load,

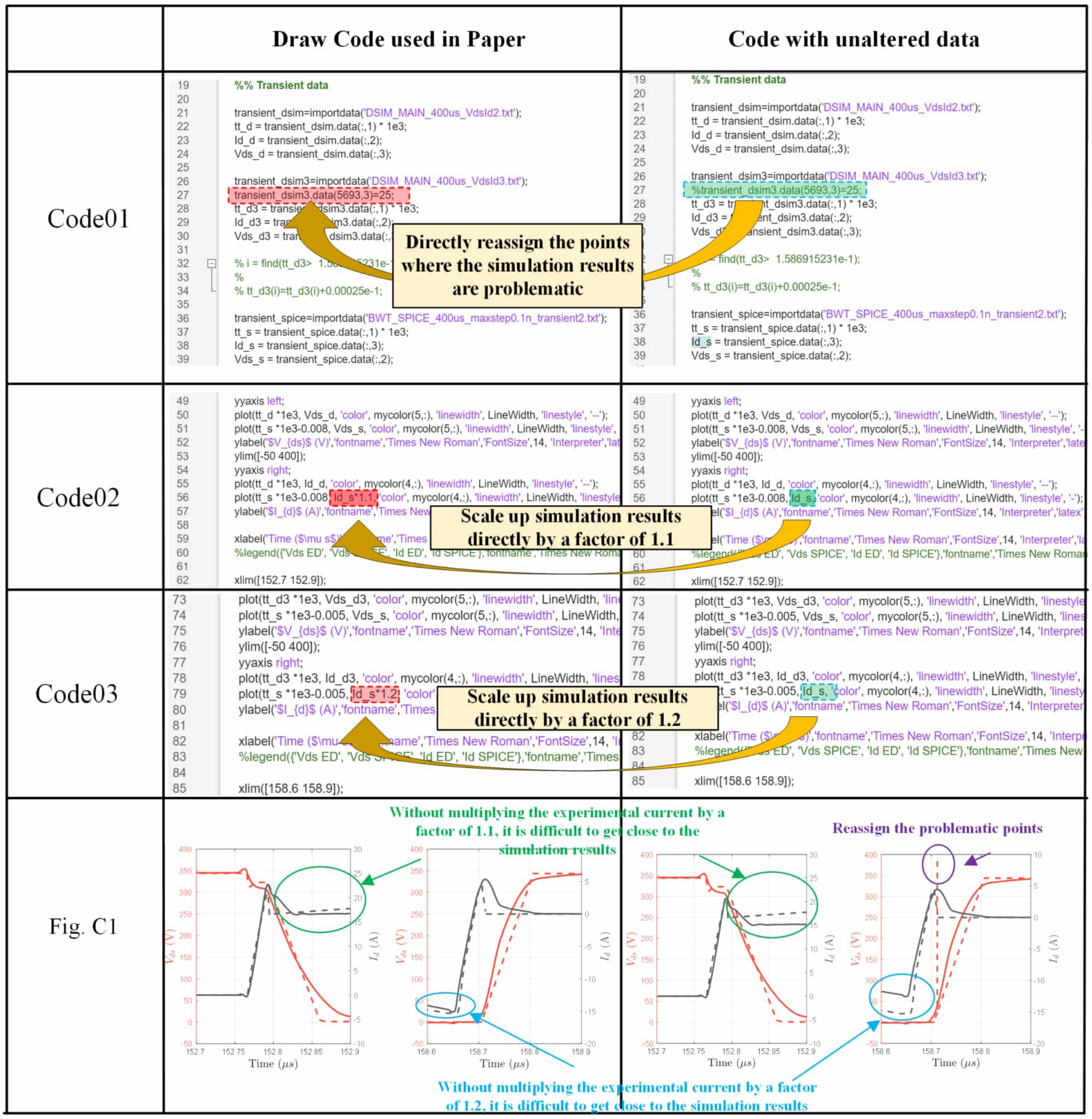
04 THSA Application Article (Q1 Journal TCAS-1)

In addition to the above three representative works, in order to quickly and effortlessly have more papers, I choose to replace the examples to water the papers. For example, this paper, Event-Driven Approach With Time-Scale Hierarchical Automaton for Switching Transient Simulation of SiC-Based High-Frequency Converter, reapplies the above PAT model to a new system. The full text of the paper can be obtained by clicking link.

Problem Overview

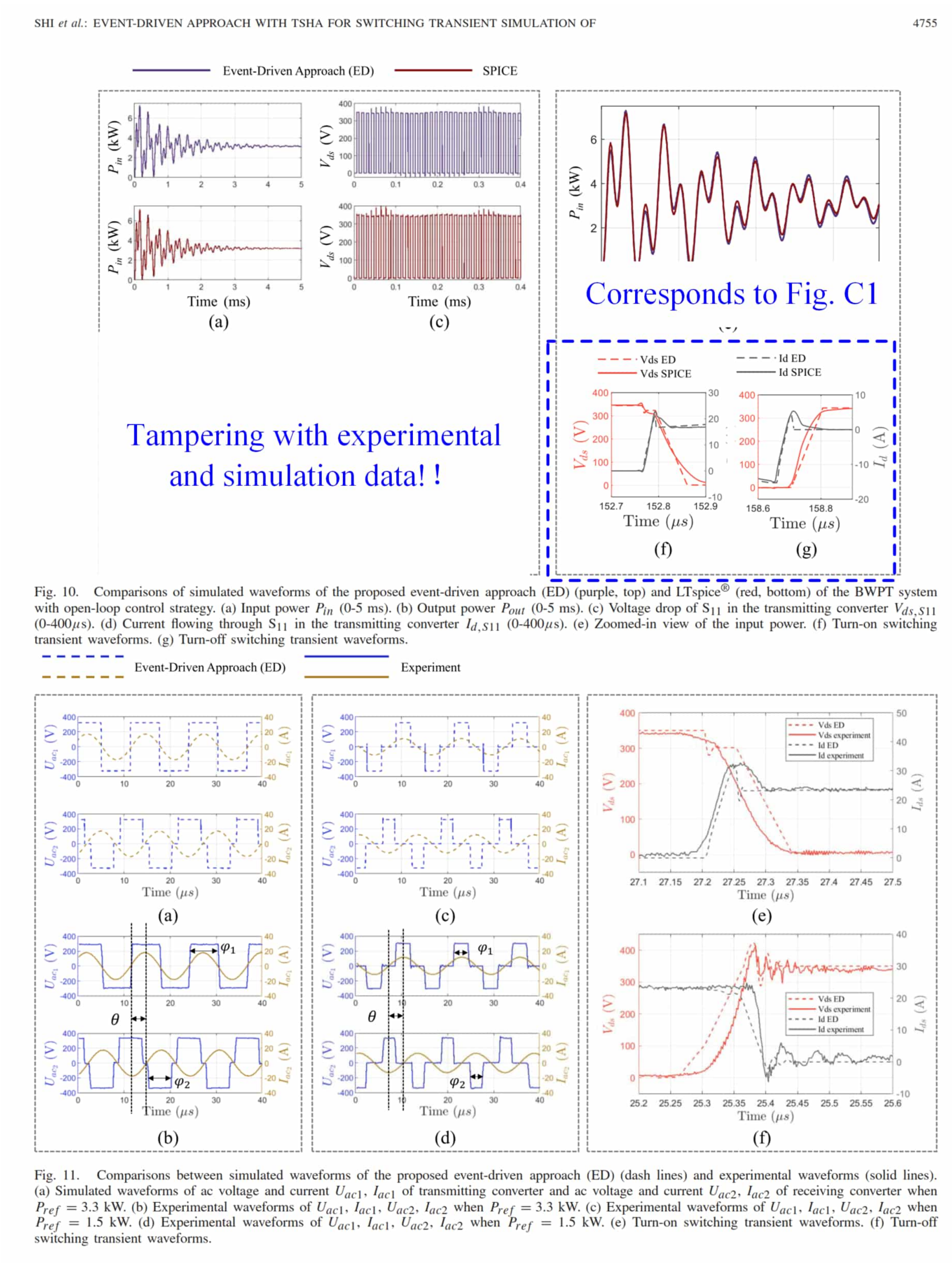
After explaining the above three core supporting articles, it is not difficult to see that if my PAT model and simulation results want to match the experiment, I can only rely on tampering with the experimental data. So this article is no exception. In order to match the PAT model with other results, I certainly also "fabricated and tampered" the simulation data. I believe that everyone has basically mastered the method of tampering with data through the above three articles. In order to save space, I will only show the "academic misconduct process" of one figure in this article below to highlight the extensiveness of my "academic misconduct".

Below, I will use Fig. 10 (f-g) in the paper as an example to explain in detail where the code is modified, and compare the results before and after the modification. The detailed data processing code and verification process can be found in Code_for_THSA.



Solution effect

Through the above efforts, I completely solved the underlying problem of the inconsistency between simulation results and experimental results in loss calculation. Furthermore, the processed data in matlab was plotted using professional drawing software. Fig. C1 corresponds to Fig. 10 (f-g) in the journal article, and it was also written in my doctoral thesis.



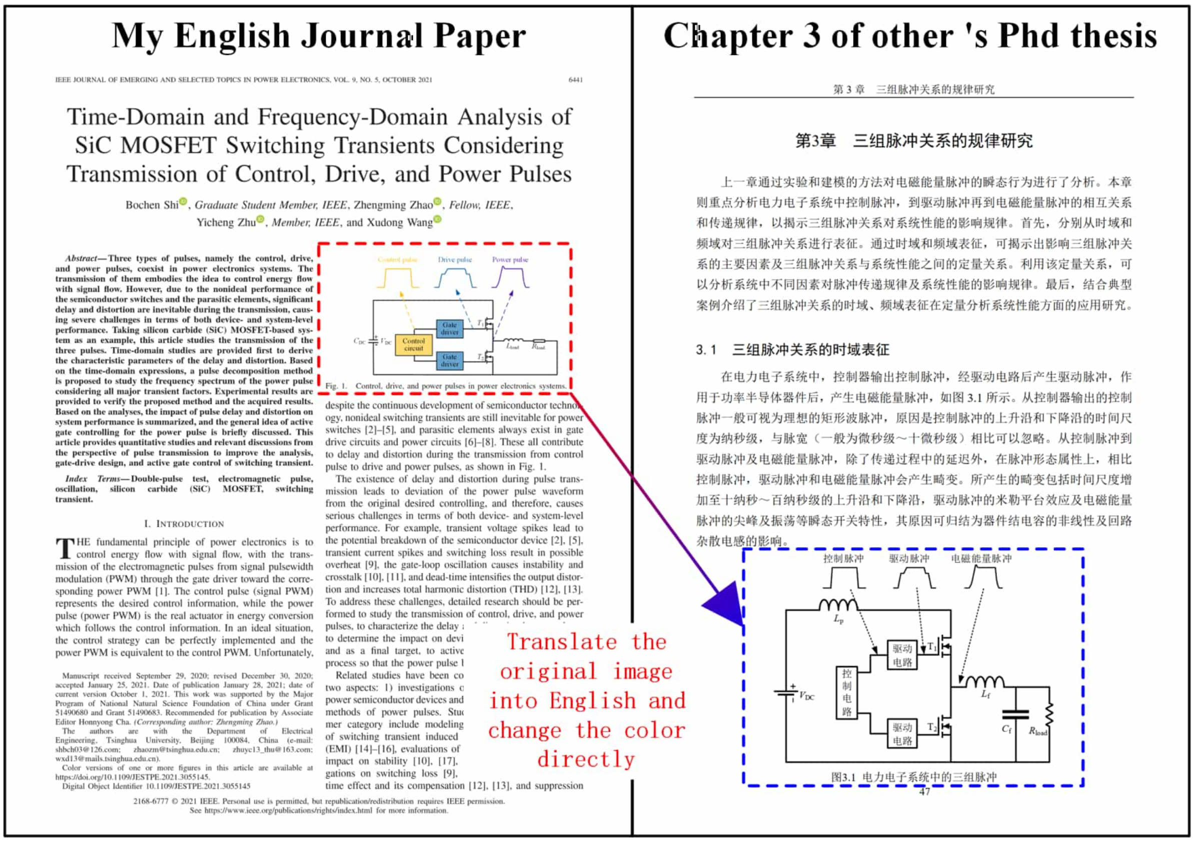
05 Three groups of pulse articles (Q1 journal JESTPE)

Problem Overview

In the above four articles, I mainly encountered the problem of **inaccurate expected results**. I believe that everyone has learned the "data fabrication and tampering" method I used (mainly including deletion, fabrication, tampering and other means of data results). Next, I will use another paper as an example to solve the second problem-the problem of **not enough paper results**. Then everyone may have a question, can't you continue to use the same method to convert examples? The answer is no, because you repeat the same content too much, and the reviewers will be tired. You see, I published in the top journals TPEL and TIE at the beginning. Later, because the reviewers of the top journals were tired, I could only publish in the inferior TCAS-1 journal, and finally I could only publish in the open source IEEE Access. So this method alone is not sustainable. Then I will teach you a little trick. Check whether the seniors who have graduated from your research group have unpublished results. If not, then this little trick is not applicable. If so, then congratulations, you can get another article. For example, I translated the third chapter of my senior's doctoral dissertation into English and published it in the journal `IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS`. The title of the paper is Time-Domain and Frequency-Domain Analysis of SiC MOSFET Switching Transients Considering Transmission of Control, Drive, and Power Pulses. The full text of the paper can be obtained by clicking [link](). The full text of my doctoral thesis can be obtained by clicking [link]().

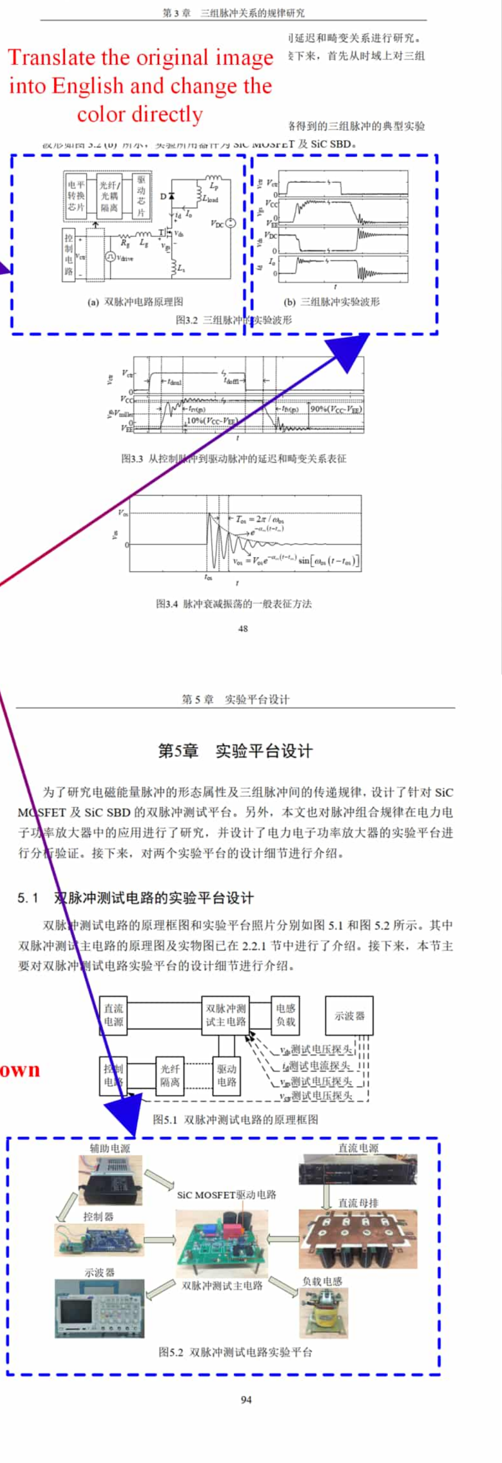
Solution effect

In order to facilitate your understanding, I will translate the [paper]() and compare it with my senior's doctoral thesis. Please bear with me if the translation is not good:

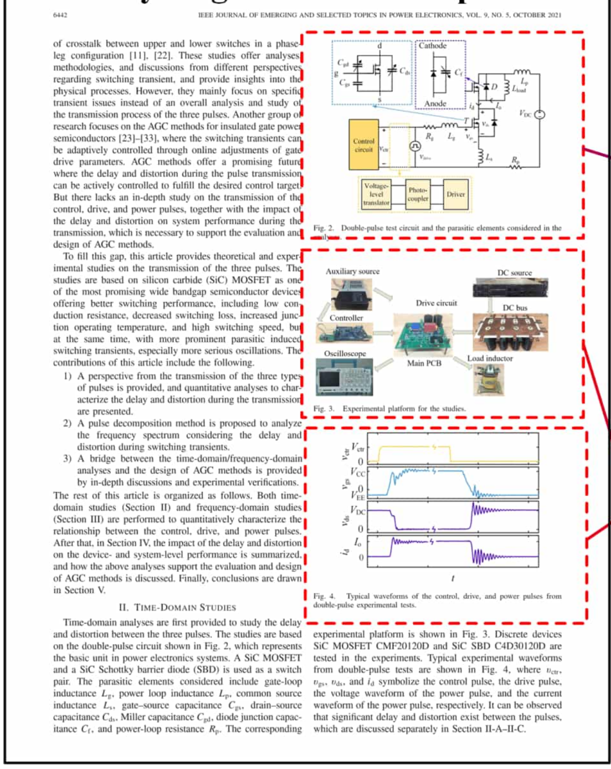


Chapter 3 of other 's Phd thesis

Translate the original image into English and change the color directly

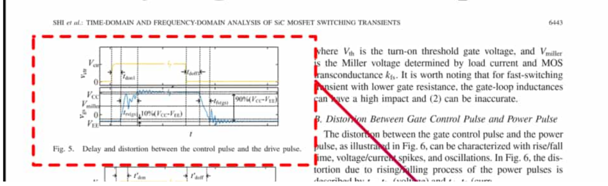


My English Journal Paper

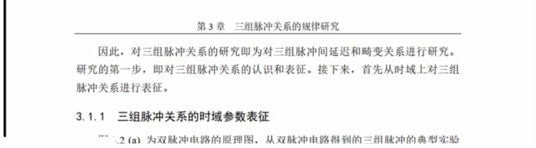


- **Cover the Chinese with a text box**
- **You don't even need to draw your own diagrams**

My English Journal Paper



Chapter 3 of other 's Phd thesis



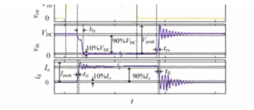


Fig. 6. Delay and distortion between the control pulse and the power pulses.

A. Delay Between Pulses

Delay between the three pulses is discussed first. The transmission from the control pulse to the drive pulse is illustrated in Fig. 5. The rise time and the fall time of the control pulse are usually of or less than the nanosecond-level time scale, and are hence ignored in this article. So the control pulse can be approximately regarded as an ideal square wave. The delay time from control to drive pulse is denoted as t_{don1} and t_{doff1} for turn-on and turn-off processes, respectively. They are mainly due to the delay of logic chips, isolation circuits (photo-coupler or optical fiber), and driving chips. t_{don1} and t_{doff1} are generally independent of the parameters in the power circuits (e.g., dc-bus voltage, load current, etc.), but instead dependent on the temperature of the chips/isolators. Experimental measurements can be performed to determine the corresponding delays.

The transmission from the control pulse to the power pulses (voltage and current) is illustrated in Fig. 6. The delay time is defined as

$$\begin{cases} t'_{don} = t_{don1} + t_{don} \\ t'_{doff} = t_{doff1} + t_{doff} \end{cases} \quad (1)$$

where t_{don} and t_{doff} are the delay time between the drive pulse and the power pulse, coinciding with the definitions in the manufacture's datasheet [34]. These delays are dependent on the gate-loop parameters. With relatively large gate resistance and relatively slower switching transients, the gate charging/discharging processes and the variations of the gate current during the delay are relatively slow. Therefore, with the assumption of ignoring the gate-loop parasitic inductances [20], analytical expressions of the delay time can be given as

$$\begin{cases} t_{don} = R_g(C_{gs} + C_{gd}(v_{ds} = V_{DC})) \ln \dfrac{V_{CC} - V_{EE}}{V_{CC} - V_{th}} \\ t_{doff} = R_g(C_{gs} + C_{gd}(v_{ds} = 0)) \ln \dfrac{V_{CC} - V_{EE}}{V_{miller} - V_{EE}} \end{cases} \quad ($$

the SiC MOSFET switching transient model expressions of the voltage fall time and the are derived as

$$\begin{cases} t_{ri} = t_{ri1} + t_{ri2} \\ t_{ri1} = \dfrac{-B_0 + \sqrt{B_0^2 - 4A_0C_0}}{2A_0} \\ t_{ri2} = \dfrac{R_g(C_{gs} + C_{gdL})(V_{miller} - V_{gs1}) + L_s I_o/2}{V_{CC} - V_{gs1}/2 - V_{miller}/2} \\ A_0 = g_{fs}(V_{CC} - V_{th}) - I_o/4 \\ B_0 = -\dfrac{I_o}{2}[g_{fs}L_s + R_g(C_{gs} + C_{gdL})] \\ C_0 = -g_{fs}R_g C_{gdL} L_s \dfrac{I_o}{2} \end{cases} \quad (3)$$

$$\begin{cases} t_{fv} = \dfrac{-B_2 \cdot \sqrt{B + \frac{2}{2} - 4A_2C_2}}{2A_2} \\ A_2 = g_{fs}\left(V_{CC} - \dfrac{V_{miller}}{2} - \dfrac{I_{peak}}{2g_{fs}} - \dfrac{V_{th}}{2}\right) \\ B_2 = -(C_{eq1}/2 + g_{fs}R_{gon}C_{gd})(V_{DC} - V_{miller} + V_{th}) \\ \quad -g_{fs}R_{gon}(C_{gs} + C_{gd})(V_{miller} - (I_L + I_o)/g_{fs} - V_{th}) \\ C_2 = -R_{gon}(C_{gs} + C_{gd})C_{eq1}(V_{DC} - V_{miller} + V_{th}) \end{cases} \quad (4)$$

where the definitions of the coefficients of the junction capacitance characteristics including C_{eq1} and C_{gdL}, and the linear transconductance coefficient of the MOSFET denoted as g_{fs}, can be found in [20]. The spikes are denoted as peak voltage V_{peak} and peak current I_{peak}. The expressions are given as [20]

$$\begin{cases} V_{peak} \approx V_{DC} + (L_s + L_p)|di/dt|_{off} \\ I_{peak} \approx I_o + \sqrt{dQ|di/dt|_{on}} \end{cases} \quad (5)$$

where dQ is the charge accumulated in C_f during the turn-on process, $|di/dt|_{on}$ and $|di/dt|_{off}$ are the average changing rate of i_d during turn-on current rising and turn-off current falling stage.

To study the oscillations, assumptions of the following discussions are clarified first. Both the studied circuit (Fig. 2) and the experimental setup in this article focus on discrete devices rather than power modules. Therefore, the more complicated parasitic elements inside the power module package, such as the middle-point inductances in multichip power modules [35] are not considered. Meanwhile, only one dc-bus capacitor ...ed to be ...plications, ...esign, and ...ions [36].

Direct use of images

Direct use of images

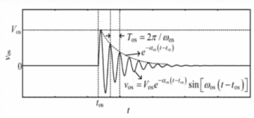


Fig. 7. General mathematical form of damped sine waveform to describe the damping ringing during switching transient.

TABLE I
CHARACTERISTIC PARAMETERS OF THE DAMPED OSCILLATIONS

	Amplitude V_{os} (I_{os})	Frequency ω_{os}	Damping α_{os}
Turn-on current oscillation	$\sqrt{dQ\|di/dt\|_{on}}$	$\sqrt{\frac{1}{L_{stray}C_f}}$	$\frac{R_p + R_{ds(on)}}{2L_{stray}}$
Turn-off voltage oscillation	$L_{stray}\|di/dt\|_{off}$	$\frac{1}{\sqrt{L_{stray}(C_{gd}+C_{ds})}}$	$\frac{R_p + R_{D(on)}}{2L_{stray}}$
Turn-off current oscillation	$(C_{gd}+C_{ds})L_{stray}\|di/dt\|_{off}$	$\frac{1}{\sqrt{L_{stray}(C_{gd}+C_{ds})}}$	$\frac{R_p + R_{D(on)}}{2L_{stray}}$

Such practical designs are not considered in the analysis for simplicity. Similarly, the load current (I_o in Fig. 2) is also considered as constant.

With the assumptions, the oscillations can be described by damped sine function. The general form is shown in Fig. 7, where V_{os} (or I_{os} for current waveform) is the amplitude, ω_{os} is the frequency, T_{os} is the time period, and α_{os} is the damping ratio. Components involved in the turn-on oscillation are the diode capacitance C_f and the power loop stray inductance, while for the turn-off oscillation, the components are MOSFET capacitance C_{gd} and C_{ds} together with the power loop stray inductance. From the equivalent circuit shown in Fig. 2, the characteristic parameters describing the oscillations can be derived and summarized in Table I, where $L_{stray} = L_p + L_s$, $R_{ds(on)}$ is the ON-state resistance of the SiC MOSFET, and $R_{D(on)}$ is the ON-state resistance of the SBD. For simplifications, the transistor in the upper switch and the diode in the lower switch are ignored here, under the direction of i_d shown in Fig. 2. If taking them into consideration, the extra junction capacitance should be added into the amplitude and frequency expressions, as described in Section III-B.

Equations (3)–(5) and Table I provide quantitative expressions of the time-domain distortion (rise/fall time, spikes, and oscillations) between the control pulse and the power (voltage and current) pulse. These expressions are derived based on the switching transient models proposed in [20], where the accuracy of the model has been experimentally verified [20, Fig. 9], which also attests to the accuracy of these expressions. To further analyze the distortion between the control and power pulses, experiments are performed to see how different parameters (junction capacitances, stray inductances, and gate drive resistances) affect the distortion (rise/fall time and voltage/current spikes). The experimental results are summarized in Fig. 8.

Generally, increasing the junction capacitances C_{gs}, C_{gd}, C_{ds}, and C_f will slow down the switching transient and therefore increase the rise/fall time of the current/voltage pulse. A difference is that increasing C_{gs} mainly leads to the suppression of the current spike, while increasing C_{gd} mainly suppr... direc... so th... affect... durin... transi... and t... And for the voltage falling, theoretically the discharging of C_{ds} will influence the fall time. The nonlinear characteristics of the junction capacitances can be the reason of a higher impact of C_{ds} on the turn-off than the turn-on transient. As for the spikes, increasing C_{ds} and C_f both help suppress the voltage spike, but meanwhile increase the current spike.

For the stray inductances introduced from device package, connections, assembling, and cables, L_p, L_s, and L_g as shown in Fig. 2 are considered and tested. The power-loop inductance L_p mainly affects the turn-off voltage spike. On the contrary, increasing the common source inductance L_s significantly increases the rise/fall time while decreases the current/voltage spikes (within the tested range of the L_s). For gate inductance L_g, the current spike increases with the increase of the gate inductance, but considering that in practical applications, the gate driver is usually close to the devices and L_g is usually around 10 nH, such an impact can be ignored.

For the gate resistance R_g, it influences the charging/discharging speed of the gate capacitors. Therefore, the rise/fall time increases with the increase of R_g, meanwhile the voltage/current spikes decrease. This large range variation of all the main parameters (time and spikes) when changing R_g offers an opportunity to actively control the switching transients by online adjusting of the gate circuits, which will be discussed in Section IV.

It is worth mentioning that the studies and experiments in this article are based on the double-pulse test circuits and the corresponding experimental platforms as shown in Figs. 2 and 3, which do not take into account some of the nonideal factors in real power converters and prototypes that may affect the transmission of the pulses. In [37], several nonideal factors in PWM inverters including the load characteristics, the long cables, the multiple phases, and the coupling between SiC MOSFET and heat sink are studied. It is highlighted that these factors potentially lead to worse switching performance, such as slower switching speed, higher switching loss, and more series oscillations, or in order words, more serious distortion between the pulses. The in-depth studies of these factors are critical to real applications, but fall beyond the scope of this article

C. Distortion Between

Similarly, for the dri... can be characterized as ...

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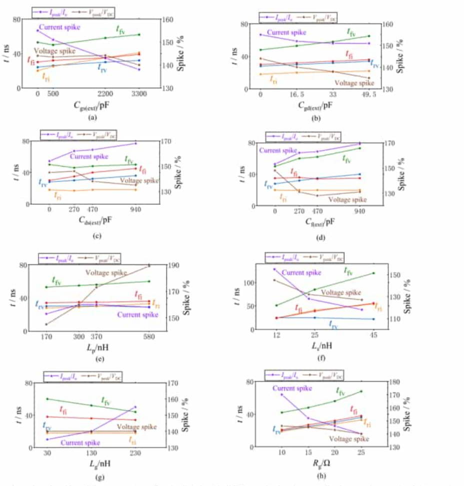

Fig. 8. Experimental results of how different parameters affect the distortion (rise/fall time and voltage/current spike) between the control and the power pulses, including (a)–(d) junction capacitances, (e)–(g) stray inductances, and (h) gate resistance.

effect, and the oscillations. For SiC MOSFET, due to smaller junction capacitance and faster switching speed, the Miller plateau is not apparent. Instead, more visible oscillations can be observed. The oscillation is of significant concern in gate drive design as it potentially leads to spurious operation of the semiconductor device, especially considering the smaller gate threshold voltage V_{th} of SiC MOSFET.

To study the drive pulse oscillations, the gate drive equivalent circuit (a portion of Fig. 2) is illustrated in Fig. 9(a). This is a single-source circuit and suitable for the study of the delay and rise/fall stages of the drive pulse, for example, the derivation of (2). However, in the oscillation stages, power loop oscillations can be coupled into the gate

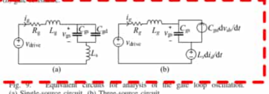

Fig. 9. Equivalent circuits for analysis of the gate loop oscillation. (a) Single-source circuit. (b) Three-source circuit.

loop through two mechanisms [18]: the Miller capacitance C_{gd} and the common source inductance L_s. A three-source circuit shown in Fig. 9(b) can be better to take these two effects into considerations. This circuit implies that even if the gate loop itself is in underdamped condition, namely

图3.2 (b) 所示，实验所用器件为 SiC MOSFET 及 SiC SBD。

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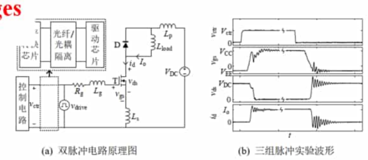


(a) 双脉冲电路原理图 (b) 三组脉冲实验波形

图3.2 三组脉冲的实验波形

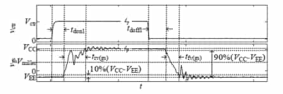


图3.3 从控制脉冲到驱动脉冲的延迟和畸变关系表征

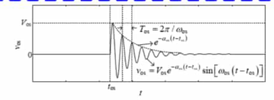


图3.4 脉冲衰减振荡的一般表征方法

$$\begin{cases} V_{peak} = V_{DC} + L_{stray}|di/dt|_{off} \\ I_{peak} \approx I_o + \sqrt{dQ|di/dt|_{on}} \end{cases} \quad (3\text{-}1)$$

4. 电压、电流振荡，同样用衰减正弦函数来表征。其参数表征如表 3.1 所示。

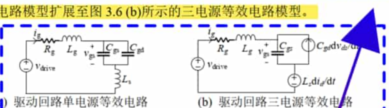
表3.1 电磁能量脉冲振荡的参数表征

	振荡幅值 V_{os}(或 I_{os})	振荡频率 ω_{os}	衰减系数 α_{os}
开通电流振荡	$\sqrt{dQ\|di/dt\|_{on}}$	$1/\sqrt{L_{stray}C_f}$	$(R_p+R_{ds(on)})/2L_{stray}$
关断电压振荡	$L_{stray}\|di/dt\|_{off}$	$1/\sqrt{L_{stray}(C_{gd}+C_{ds})}$	$(R_p+R_{D(on)})/2L_{stray}$
关断电流振荡	$(C_{gd}+C_{ds})L_{stray}\|di/dt\|_{off}$	$1/\sqrt{L_{stray}(C_{gd}+C_{ds})}$	$(R_p+R_{D(on)})/2L_{stray}$

3.1.2 驱动脉冲的振荡行为分析

在上一章中，以 SiC MOSFET 为对象提出了开关瞬态分析模型，通过该模型可以对上述三组脉冲的主要延迟和畸变关系进行定量分析。然而，为了简化模型计算，所提分析模型并未考虑驱动脉冲 v_{gs} 的振荡。考虑到驱动脉冲的振荡在 SiC MOSFET 开关过程中更为显著，容易引起开关器件误动作，进而引入稳定性问题，所以，接下来重点对 SiC MOSFET 中驱动脉冲的振荡现象进行分析。

同样以图 3.2 (a)所示的双脉冲测试电路作为研究对象，与驱动脉冲有关的等效电路如图 3.6 (a)所示，称为驱动脉冲的单电源等效电路模型。考虑到该模型并未考虑主电路对驱动脉冲产生影响，即 $C_{gd}dv_{ds}/dt$ 效应和 $L_s di_d/dt$ 效应，因此需要将单电源等效电路模型扩展至图 3.6 (b)所示的三电源等效电路模型。



(a) 驱动回路单电源等效电路 (b) 驱动回路三电源等效电路

图3.6 驱动脉冲的等效电路模型

由三电源等效电路可知，当电磁能量脉冲发生电压振荡或电流振荡时，会通过 $C_{gd}dv_{ds}/dt$ 及 $L_s di_d/dt$ 效应，将振荡引入驱动回路，进而引起驱动电压振荡。因此结合等效电路分析，可以得到开通和关断过程中 v_{gs} 振荡阶段的时域参数，如(3-2)和(3-3)所示。

Chinese-English translation (the most demanding part of the workload)

为了研究驱动脉冲振荡，栅极驱动等效电路（图2的一部分）如 图9（a）所示。这是一个单源电路，适用于研究驱动脉冲的延迟和上升/下降阶段，例如（2）的推导。然而，在振荡级中，电源环路振荡可以通过两种机制耦合到栅极环路 中[18]：米勒电容C_{gd} 和公共源电感L_s .图9（b）所示的三源电路可以更好地考虑这两种效应。该电路意味着，即使栅极环路本身处于欠阻尼状态，即 $R_g^2(C_{gs}+C_{gd}) > 4L_g$，电源环路振荡仍可通过 C_{gd} 和L_s 进入栅极环路（这通常是导致驱动脉冲振荡的主要因素），因此威胁到稳定性。

$R_g^2(C_{gs}+C_{gd}) > 4L_g$, the power loop oscillations can still be introduced through C_{gd} and L_s into the gate loop (which is more often than not the dominating factor contributing to the drive pulse oscillations) and therefore threaten the stability.

SPICE simulations and double-pulse experiments are performed with Cree SiC MOSFET CMF20120D and SiC SBD C4D30120D to study the impact of different gate drive parameters on gate pulse oscillations. As shown in Fig. 10, the simulated and experimental results are not perfectly identical but they exhibit consistent trends. In general, the amplitude of the oscillation decreases with the increase of R_g and C_{gs}, while it increases with the increase of C_{gd}. However, the increase of L_s has a limited impact on the oscillations due to two opposite effects: decreased V_{os} and I_{os} of the power pulse, while increased L_s hence stronger coupling between the gate and power loop ($L_s di/dt$). Comprehensively speaking, the variation of L_s has a restricted impact on the suppression of gate pulse oscillation. Based on these results, from the perspective of gate-loop design, increasing R_g, adopting SiC MOSFET with higher C_{gs}/C_{gd} ratio, or adding external paralleled gate–source capacitance are effective approaches to suppress the drive pulse oscillations and avoid spurious operations of the device.

翻译：使用Cree SiC MOSFET CMF20120D和SiC SBD C4D30120D进行SPICE仿真和双脉冲实验，以研究不同栅极驱动参数对栅极脉冲振荡的影响。如图10所示，仿真结果和实验结果并不完全相同，但趋势一致。一般来说，振荡的幅度随着Rg 和Cgs ，而它随着Cgd .然而，增加Ls 由于两个相反的效应，对振荡的影响有限： 降低Vos 和Ios 的功率脉冲，同时增加Ls 因此，栅极和电源环路之间的耦合更强（Lsdi/dt）.综合来说，变化Ls 对栅极脉冲振荡的抑制影响有限。基于这些结果，从门环设计的角度来看，增加Rg ，采用SiC MOSFET更高Cgs/Cgd 比率或增加外部并联栅源电容是抑制驱动脉冲振荡和避免器件杂散操作的有效方法。

where R represents $R_{ds(...)}$ ... 25 °C, T_{J1} and T_{J2} are tw... device datasheet. The co... the equations of (7) and (... curves from the device d... between T_J and device pa...

Tips：可以直接将博士论文中图的中文用英文文本框盖住（盖住部分与原图的清晰度不同）

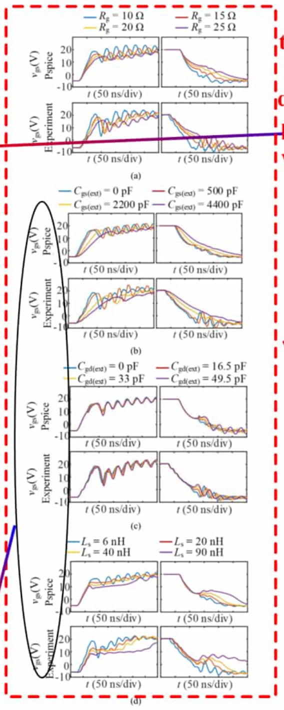


Fig. 10. Comparisons of drive pulses under different gate drive parameters. The turn-on transient is ON the left, and the turn-off ON the right. (a) Impact of R_g. (b) Impact of C_{gs}. (c) Impact of C_{gd}. (d) Impact of L_s.

III. Frequency-Domain Studies

In Section II, the time-domain expressions of the power pulses are derived, including delay (described by delay time) and distortion (described by rise/fall time and damping sine functions). Based on the time-domain expressions, frequency-domain studies can be performed to investigate the frequency-related performance such as output THD and EMI. A pulse decomposition method is proposed in this section to quantitatively study the frequency-domain characteristics of the power pulses, considering all major impacts during switching transient including dead-time, delay, rise/fall, and oscillation. With the frequency-domain studies, more comprehensive

Chinese-English translation (the most demanding part of the workload)

从公式(3-2)和(3-3)可以看出，驱动脉冲振荡的频率和衰减系数与电磁能量脉冲的振荡过程一致，而振荡幅值则受电磁能量脉冲振荡幅值 I_{os} 或 V_{os},及驱动回路参数 R_g, C_{gs}, C_{gd} 及 L_s 影响。通过 Pspice 仿真及双脉冲实验结果，图 3.7 展示了主要驱动回路参数 R_g, C_{gs}, C_{gd} 及 L_s 对驱动脉冲振荡过程的影响。可以看到，在驱动脉冲的波形轨迹上，仿真和实验结果存在一定的偏差。这主要是由于实验测量结果受探头引入的杂散电感及器件内部栅极和源极杂散电感影响，而 PSpice 仿真结果并未考虑这一因素。而从影响规律方面，仿真和实验结果相一致，即驱动脉冲的振荡幅值随着 C_{gd} 的增加而增加，随着 R_g 及 C_{gs} 的增加而减小。而 L_s 主要从两方面影响驱动脉冲的振荡幅值。一方面，增加 L_s，会抑制开关过程中的 di/dt，进而抑制电磁能量脉冲的振荡幅值 I_{os} 和 V_{os}。另一方面，增加 L_s，也会使 $L_s dI_d/dt$ 效应对驱动脉冲振荡的影响更显著。综合两方面因素，通过改变 L_s 对驱动振荡脉冲进行抑制的效果有限。

因此，通过对驱动回路的振荡过程进行等效电路分析，揭示了影响驱动回路振荡幅值的主要参数，并结合仿真和实验分析，总结了主要驱动回路参数对驱动电压振荡过程的影响规律。从设计层面，为了提高驱动稳定性角度，增加 R_g，选择高 C_{gs}/C_{gd} 比例的 SiC MOSFET 或者在栅源极并联外部电容，是抑制驱动回路振荡的有效方法。

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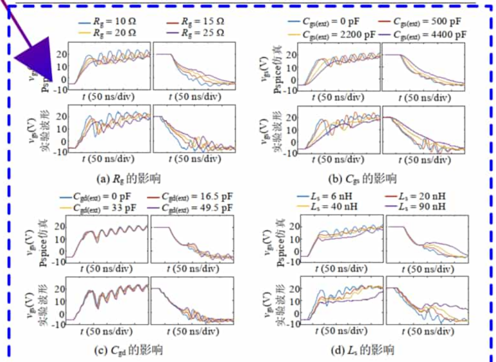

图3.7 驱动脉冲的波形对比（左边开通过程，右边关断过程）

3.2 三组脉冲关系的频域表征

在上一节中，从时域上对三组脉冲形态属性关系进行了定量表征，同时也将三组脉冲关系与系统性能（如电压、电流应力，开关损耗）联系起来。然而其他性能如系统输出 THD、EMI 等性能则与脉冲的频域特征有关。为了更全面地分析三组脉冲规律与系统性能之间的相互关系，本节重点分析控制脉冲与电磁能量脉冲在频域上的关系，在此基础上，分析不同延迟和畸变关系对于电磁能量脉冲频谱和系统性能的影响规律。

分析对象为半桥电路，所比较的控制脉冲和电磁能量脉冲如图 3.8 所示。将两个脉冲进行归一化处理后，所比较的控制脉冲可视为理想电磁能量脉冲。而所研究的实际电磁能量脉冲选择为桥臂输出脉冲，即桥臂下管的管压降，用 v_{leg} 表示，相应的频域表达式为 $V_{leg}(f)$. 桥臂输出脉冲序列的频谱特性会受调制频率 T_0, 开关频率 T_s, 占空比 D, 死区 t_d，开通关断延迟和开关过渡过程（包括电压上升和下降时间及电压振荡）的影响。

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分析的控制脉冲和功率脉冲如图11所示。控制脉冲vctr 可以算是理想的方波。所研究的功率脉冲是半桥的输出电压脉冲，即下部开关的漏源电压，表示为vleg 在时域和Vleg(f) 在频域中。其频谱取决于调制频率f0 、开关频率fs （切换周期Ts=1/fs ）、占空比D 、死区时间td 、导通/关断延迟、上升/下降时间和电压振荡。

在现有文献中，类似的方法已被用于分析有死区的PWM脉冲和PWM脉冲[39]，但忽略了开关瞬态。在以下各部分中，综合考虑了死区时间、延迟时间和瞬态过程，以研究输出电压脉冲的频谱。为方便起见，控制脉冲和功率脉冲经过归一化。

Chinese-English translation

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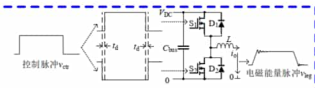

图3.8 频域分析的研究对象

目前对脉冲进行频域分析的方法主要有直接 FFT 分析法，双重傅里叶积分法和脉冲分解法。其中直接 FFT 分析法需要首先通过仿真建模得到脉冲波形，再通过 FFT 计算其频谱。该方法简化了求解频谱过程的数学推导，但仿真建模及 FFT 计算都会影响求解速度，计算精度也受仿真步长的影响。双重傅里叶积分法适合于分析周期性调制所得到脉冲的频谱，其相较于 FFT 计算的优点是提供脉冲频谱的解析解，但其缺点是通用性不强[92]。而脉冲分解法是通过将脉冲进行分解，求分解后各个脉冲的傅里叶变换，叠加得到整个脉冲的频谱，是一种对脉冲频谱的直接计算方法，不依赖于周期性调制方法，通用性更强[92]。基于脉冲分解的频域

Chinese-English translation

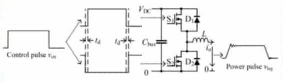

Fig. 11. Studied control pulse and power pulse in frequency-domain studies.

analyses regarding the relationship between the control and power pulses, and between the transmission delay/distortion and system performance can be provided.

The analyzed control pulse and power pulse are illustrated in Fig. 11. The control pulse v_{co} can be regarded as an ideal square wave. The studied power pulse is the output voltage pulse of the half bridge, namely the drain–source voltage of the lower switch, denoted as v_{leg} in time-domain and $V_{leg}(f)$ in frequency-domain. Its frequency spectrum is dependent on modulation frequency f_0, switching frequency f_s (switching period $T_s = 1/f_s$), duty cycle D, dead-time t_d, turn-on/off delay, rise/fall time, and voltage oscillation. Here we only focus on PWM and assume a constant switching frequency of the converter for simpler derivations of the frequency-domain analytical expressions. Other modulations such as pulse frequency modulation (PFM) and pulse amplitude modulation (PAM) and more advanced variable-frequency control strategies are beyond the scope of this article.

The studies are performed based on pulse decomposition, guaranteed by the linearity of the Fourier transformation, as shown in the following equation:

$$\mathcal{F}\left[\sum_{i=1}^{N} A_i f_i(t)\right] = \sum_{i=1}^{N} A_i F_i(\omega). \quad (9)$$

In the available literature, similar methods have been used to analyze idea PWM pulses and PWM pulses with dead-time [39], however, ignoring the switching transient. In the following parts, dead-time, delay time, and transient process are comprehensively considered to study the frequency spectrum of the output voltage pulse. The control and power pulses are normalized for convenience.

A. Frequency Spectrum of Ideal Power Pulse

When ignoring dead-time, delay, and switching transient, namely, studying an ideal power pulse, the frequency spectrum will be identical to that of the control pulse. Such a situation is studied first in this section. A PWM pulse, taking trailing-edge PWM (TEPWM) as an example [40], can be decomposed into a square wave with 50% duty cycle, defined as $p_{c,TE}$, plus a pulse sequence related to the modulation signal, defined as $p_{s,TE}$

$$v_{leg,TE}(t) = p_{c,TE}(t) + p_{s,TE}(t). \quad (10)$$

The time-domain and frequency-domain expressions of $p_{c,TE}$ are given as

$$p_{c,TE}(t) = \sum_{k=-\infty}^{\infty} [u(t-kT_s) - u(t-kT_s-T_s/2)] \quad (11)$$

$$p_{c,TE}(f) = \sum_{k=-\infty}^{\infty} \frac{2}{j(2k+1)} \delta[f-(2k+1)f_s] + \pi\delta(f) \quad (12)$$

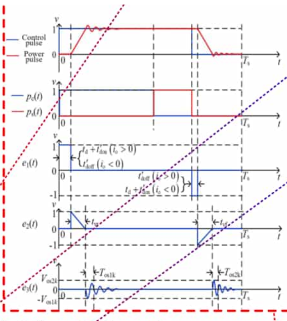

Fig. 12. Decomposition of the power pulse.

where u is the unit step function and δ is the unit impulse function. The time-domain and frequency-domain expressions of $p_{s,TE}$ are given as

$$p_{s,TE}(t) = \sum_{k=-\infty}^{\infty} \left[u\left(t-kT_s-\frac{1}{2}T_s\right) - u(t-kT_s-\tau_k)\right] \quad (13)$$

$$p_{s,TE}(f) = \begin{cases} \sum_{k=-\infty}^{\infty} \frac{2}{-j2\pi f}\left[e^{-j2\pi f(kT_s+\tau_k)} - e^{-j2\pi f(kT_s+1/2T_s)}\right], & f \neq 0 \\ \sum_{k=-\infty}^{\infty}\left(\tau_k - \frac{T_s}{2}\right), & f = 0 \end{cases} \quad (14)$$

where τ_k is the pulsewidth of the PWM pulse in the kth period. Then the frequency spectrum of ideal power pulse can be calculated with

$$v_{leg,TE}(f) = p_{c,TE}(f) + p_{s,TE}(f). \quad (15)$$

B. Frequency Spectrum of Real Power Pulse

The impact of dead-time and delay, rise/fall time, and oscillation in real power pulse can be described with $e_1(t)$, $e_2(t)$, and $e_3(t)$, respectively, as shown in Fig. 12. $e_1(t)$ is a rectangular pulse between ±1 describing dead-time and delay. $e_2(t)$ is a sawtooth pulse between ±1 describing rise/fall time. $e_3(t)$ is a damping sine pulse describing oscillation.

Considering all these nonideal factors, the final expression of the output voltage pulse is given as

$$v_{leg,TE}(t) = p_{c,TE}(t) + p_{s,TE}(t) - e_{1,TE}(t) - e_{2,TE}(t) - e_{3,TE}(t). \quad (16)$$

当忽略死区时间、延迟和开关瞬态时，即研究理想功率脉冲时，频谱将与控制脉冲的频谱相同。本节首先研究这种情况。以后沿PWM（TEPWM）为例[40]，PWM脉冲可以分解为占空比为50%的方波，定义为pc,TE ，加上与调制信号相关的脉冲序列，定义为ps,TE

时域和频域表达式pc,TE 给出为

哪里u 是单位步进函数，并且δ 是单位脉冲函数。时域和频域表达式ps,TE 给出为：

哪里τk 是 PWM 脉冲的脉冲宽度k 第期。然后可以计算出理想功率脉冲的频谱

死区时间和延迟、上升/下降时间和有功功率脉冲振荡的影响可以用e1(t) ,e2(t) 和e3(t) ，如图12所示。e1(t) 是介于 ±1 之间的矩形脉冲，用于描述死区时间和延迟。e2(t) 是介于 ±1 之间的锯齿脉冲，描述上升/下降时间。e3(t) 是描述振荡的阻尼正弦脉冲。

考虑到所有这些非理想因素，输出电压脉冲的最终表达式为

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分析方法是利用了傅里叶变换的线性特性[93]，如(3-4)所示。

$$\mathcal{F}\left[\sum_{i=1}^{N} A_i f_i(t)\right] = \sum_{i=1}^{N} A_i F_i(\omega) \quad (3\text{-}5)$$

目前，已有文献基于脉冲分解法，主要对理想 PWM 脉冲[94]及含有死区的 PWM 脉冲[92]频谱进行了分析，并未考虑脉冲间延迟和畸变的影响。接下来，本节将以半桥电路输出电磁能量脉冲序列为研究对象，综合考虑死区、延迟及开关过渡过程对输出脉冲频谱的影响。为了简化分析，对输出脉冲序列进行归一化处理，即认为输出脉冲的幅值在 0，1 之间。

3.2.1 理想电磁能量脉冲的频谱分析

不考虑死区、延迟和开关过渡过程时，理想电磁能量的频谱特性和控制脉冲的频谱特性一致。对任意一 PWM 信号，可分解为占空比为 50%的方波信号叠加一个与调制信号有关的脉冲序列[94]。以下降沿单边调制 PWM (Trailing-edge PWM, TEPWM)为例，进行分析。有

$$v_{leg,TE}(t) = p_{c,TE}(t) + p_{s,TE}(t) \quad (3\text{-}6)$$

其中 $p_c(t)$的表达式及其傅里叶变换为

$$p_{c,TE}(t) = \sum_{k=-\infty}^{\infty}\left[u(t-kT_s) - u(t-kT_s-T_s/2)\right] \quad (3\text{-}7)$$

$$P_{c,TE}(f) = \sum_{k=-\infty}^{\infty}\frac{2}{j(2k+1)}\delta\left[f-(2k+1)f_s\right] + \pi\delta(f) \quad (3\text{-}8)$$

与调制信号有关的项 $p_{s,TE}(t)$的表达式和傅里叶变换为

$$p_{s,TE}(t) = \sum_{k=-\infty}^{\infty}\left[u\left(t-kT_s-\frac{1}{2}T_s\right) - u\left(t-kT_s-\tau_k\right)\right] \quad (3\text{-}9)$$

$$P_{s,TE}(f) = \begin{cases}\sum_{k=-\infty}^{\infty}\frac{1}{-j2\pi f}\left[e^{-j2\pi f(kT_s+\tau_k)} - e^{-j2\pi f(kT_s+T_s/2)}\right], f \neq 0 \\ \sum_{k=-\infty}^{\infty}\left(\tau_k - \frac{T_s}{2}\right), f = 0\end{cases} \quad (3\text{-}10)$$

其中 τ_k 为第 k 个开关周期的控制脉冲的脉宽。因此，对于一般性的调制信号，理想电磁能量脉冲的频谱为

$$V_{leg,TE}(f) = P_{c,TE}(f) + P_{s,TE}(f) \quad (3\text{-}11)$$

3.2.2 实际电磁能量脉冲的频谱分析

与理想电磁能量脉冲相比，实际电磁能量脉冲要考虑死区、延迟及开关过渡过程的影响。分别用脉冲 $e_1(t)$, $e_2(t)$和 $e_3(t)$来表征这些非理想因素的影响，如图 3.9 所示。其中 $e_1(t)$是由死区和延迟引起，幅值为 ±1 的矩形波脉冲序列，$e_2(t)$是由电压上升、下降时间引起，幅值为 ±1 的锯齿波脉冲序列，$e_3(t)$是由电压振荡引起的衰减正弦脉冲序列。考虑这些非理想因素后，最终得到的桥臂输出电压

$$v_{leg,TE}(t) = p_{c,TE}(t) + p_{s,TE}(t) - e_{1,TE}(t) - e_{2,TE}(t) - e_{3,TE}(t) \quad (3\text{-}12)$$

对 $e_{1,TE}(t)$求其傅里叶变换，得到

$$E_{1,TE}(f) = \begin{cases}\sum_{k=-\infty}^{\infty}\frac{1}{-j2\pi f}\left[e^{-j2\pi f(t_{10}+\Delta t_{1k})} - e^{-j2\pi f t_{10}} - e^{-j2\pi f(t_{20}+\Delta t_{2k})} + e^{-j2\pi f t_{20}}\right], f \neq 0 \\ \sum_{k=-\infty}^{\infty}\left(\Delta t_{1k} - \Delta t_{2k}\right), f = 0\end{cases} \quad (3\text{-}13)$$

其中 $t_{10} = kT_s$, $t_{20} = kT_s+\tau_k$. Δt_{1k} 和 Δt_{2k} 的表达式如(3-14)所示。$\sigma(t)$是选择函数，即 $\sigma(t)=1(i_o(t)>0)$，否则 $\sigma(t)=0$。

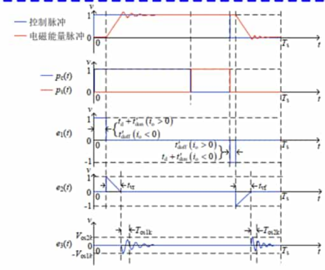

图3.9 电磁能量脉冲的分解图示

$$\begin{cases}\Delta t_{1k} = t'_{doff} + \sigma(t_{10})(t_d + t'_{don} - t'_{doff}) \\ \Delta t_{2k} = t_d + t'_{don} + \sigma(t_{20})(t'_{doff} - t_d - t'_{don})\end{cases} \quad (3\text{-}14)$$

对 $e_2(t)$求其傅里叶变换，得到

$$E_{2,TE}(f) = \begin{cases}\sum_{k=-\infty}^{\infty} e^{-j2\pi f t_{1k}}\left(\frac{1-j2\pi f t_{rk} - e^{-j2\pi f t_{rk}}}{4\pi^2 f^2 t_{rk}}\right) - e^{-j2\pi f t_{2k}}\left(\frac{1-j2\pi f t_{fk} - e^{-j2\pi f t_{fk}}}{4\pi^2 f^2 t_{fk}}\right), f \neq 0 \\ \sum_{k=-\infty}^{\infty}\left(t_{rk} - t_{fk}\right), f = 0\end{cases}$$

(3-15)

其中 t_{1k} 和 t_{2k} 分别为第 k 个开关周期内，桥臂输出电压脉冲的上升沿和下降沿起始时刻。有 $t_{1k} = t_{10}+\Delta t_{1k}$, $t_{2k} = t_{20}+\Delta t_{2k}$. t_{rk} 和 t_{fk} 分别表示该开关周期内的电压上升和下降时间。

对于 $e_3(t)$, 首先分析上升沿和下降沿两处振荡的参数表达式。脉冲上升沿的振荡是来自回路杂散电感 L_{stray} 和下管结电容 $C_{oss2}+C_{f2}$ 的串联谐振，因此有归一化后的 $V_{os1k} = V_{peak2k}/V_{DC} - 1$, 其中 V_{peak2k} 为下管关断时电压的尖峰值。振荡频率为 $\omega_{os1} = 1/\sqrt{L_{stray}(C_{oss2}+C_{f2})}$，衰减系数 $\alpha_1 = R_p/2/L_{stray}$（这里忽略了桥臂上管的导通电阻）。而脉冲下降沿的振荡发生在 L_{stray} 和上管结电容的串联谐振，此时下管呈导通状态，

3.2.2 实际电磁能量脉冲的频谱分析

与理想电磁能量脉冲相比，实际电磁能量脉冲要考虑死区、延迟及开关过渡

过程的影响。分别用脉冲 $e_1(t)$, $e_2(t)$和 $e_3(t)$来表征这些非理想因素的影响，如图 3.9 所示。其中 $e_1(t)$是由死区和延迟引起，幅值为 ±1 的矩形波脉冲序列，$e_2(t)$是由电压上升、下降时间引起，幅值为 ±1 的锯齿波脉冲序列，$e_3(t)$是由电压振荡引起的衰减正弦脉冲序列。考虑这些非理想因素后，最终得到的桥臂输出电压

$$v_{\mathrm{leg,TE}}(t)=p_{\mathrm{c,TE}}(t)+p_{\mathrm{s,TE}}(t)-e_{\mathrm{1,TE}}(t)-e_{\mathrm{2,TE}}(t)-e_{\mathrm{3,TE}}(t) \tag{3-12}$$

对 $e_{1,\mathrm{TE}}(t)$求其傅里叶变换，得到

$$E_{\mathrm{1,TE}}(f)=\begin{cases}\sum_{k=-\infty}^{\infty}\frac{1}{-j2\pi f}\left[e^{-j2\pi f(t_{10}+\Delta t_{1k})}-e^{-j2\pi f t_{10}}-e^{-j2\pi f(t_{20}+\Delta t_{2k})}+e^{-j2\pi f t_{20}}\right], f\neq 0\\ \sum_{k=-\infty}^{\infty}\left(\Delta t_{1k}-\Delta t_{2k}\right), f=0\end{cases} \tag{3-13}$$

其中 $t_{10}=kT_s$, $t_{20}=kT_s+\tau_k$. Δt_{1k}和 Δt_{2k}的表达式如(3-14)所示。$\sigma(t)$是选择函数，即 $\sigma(t)=1(i_o(t)>0)$，否则 $\sigma(t)=0$。

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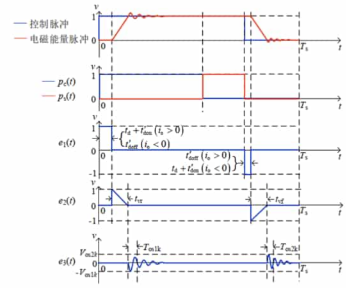


图3.9 电磁能量脉冲的分解图示

$$\begin{cases}\Delta t_{1k}=t'_{\mathrm{doff}}+\sigma(t_{10})(t_{\mathrm{d}}+t'_{\mathrm{don}}-t'_{\mathrm{doff}})\\ \Delta t_{2k}=t_{\mathrm{d}}+t'_{\mathrm{don}}+\sigma(t_{20})(t'_{\mathrm{doff}}-t_{\mathrm{d}}-t'_{\mathrm{don}})\end{cases} \tag{3-14}$$

对 $e_2(t)$求其傅里叶变换，得到

$$E_{\mathrm{2,TE}}(f)=\begin{cases}\sum_{k=-\infty}^{\infty}e^{-j2\pi f t_{1k}}\left(\frac{1-j2\pi f t_{rk}-e^{-j2\pi f t_{rk}}}{4\pi^2 f^2 t_{rk}}\right)-e^{-j2\pi f t_{2k}}\left(\frac{1-j2\pi f t_{fk}-e^{-j2\pi f t_{fk}}}{4\pi^2 f^2 t_{fk}}\right), f\neq 0\\ \sum_{k=-\infty}^{\infty}\left(t_{rk}-t_{fk}\right), f=0\end{cases} \tag{3-15}$$

其中 t_{1k}和 t_{2k}分别为第 k 个开关周期内，桥臂输出电压脉冲的上升沿和下降沿起始时刻。有 $t_{1k}=t_{10}+\Delta t_{1k}$, $t_{2k}=t_{20}+\Delta t_{2k}$. t_{rk}和 t_{fk}分别表示该开关周期内的电压上升和下降时间。

对于 $e_3(t)$，首先分析上升沿和下降沿两处振荡的参数表达式。脉冲上升沿的振荡是来自回路杂散电感 L_{stray}和下管结电容 $C_{\mathrm{oss2}}+C_{\mathrm{f2}}$的串联谐振，因此有归一化后的 $V_{\mathrm{os1}k}=V_{\mathrm{peak2}k}/V_{\mathrm{DC}}-1$，其中 $V_{\mathrm{peak2}k}$为下管关断时电压的尖峰值。振荡频率为 $\omega_{\mathrm{os1}}=1/\sqrt{L_{\mathrm{stray}}\left(C_{\mathrm{oss2}}+C_{\mathrm{f2}}\right)}$，衰减系数 $\alpha_1=R_{\mathrm{p}}/2/L_{\mathrm{stray}}$（这里忽略了桥臂上管的导通电阻）。而脉冲下降沿的振荡发生在 L_{stray}和上管结电容的串联谐振，此时下管呈导通状态，

因此可认为 $V_{\mathrm{os2}k}\approx 0$. 因此，可只分析上升沿处的电压振荡。求其傅里叶变换得到

$$E_{\mathrm{3,TE}}(f)=\sum_{k=-\infty}^{\infty}-\frac{V_{\mathrm{os1}k}\omega_{\mathrm{os1}}e^{-j2\pi f(t_{1k}+t_{rk})}}{\left(\alpha_1+j2\pi f\right)^2+\omega_{\mathrm{os1}}^2} \tag{3-16}$$

因此，对于一般性调制信号，实际电磁能量脉冲的频谱为

$$V_{\mathrm{leg,TE}}(f)=P_{\mathrm{c,TE}}(f)+P_{\mathrm{s,TE}}(f)-E_{\mathrm{1,TE}}(f)-E_{\mathrm{2,TE}}(f)-E_{\mathrm{3,TE}}(f) \tag{3-17}$$

3.2.3 周期调制信号分析

以上分析针对的是一般调制信号下电磁能量脉冲频谱的计算方法，当调制信号为周期信号时，可只对一个调制周期内的信号进行分析。设调制信号周期为 T_0, 载波周期为 T_s,且有 $T_0=mT_s$, 其中 m 为整数。对于 m 为非整数情况，可以按 $pT_0=qT_s$ 处理，其中 p,q 为整数。此时，对于一般性的周期调制信号，有电磁能量脉冲频谱的计算式为

$$V_{\mathrm{leg,TE(P)}}(f)=P_{\mathrm{c,TE}}(f)+P_{\mathrm{s,TE(P)}}(f)-E_{\mathrm{1,TE(P)}}(f)-E_{\mathrm{2,TE(P)}}(f)-E_{\mathrm{3,TE(P)}}(f) \tag{3-18}$$

其中周期性调制信号频谱可由非周期信号频谱计算得到，即

$$F_{(\mathrm{P})}(f)=\frac{2\pi}{pT_0}\sum_{i=-\infty}^{\infty}F(f)\big|_{f=if_0}\delta(f-if_0) \tag{3-19}$$

其中 $F(f)$代表公式(3-10)，(3-13)，(3-15)及(3-16)，在周期信号调制时，$F(f)$中的 k 的取值为 0～q−1. 其中当 m 为整数时，有 $p=1$, $q=m$.

3.2.4 仿真及实验验证

以正弦波调制信号 $x(t)=M\sin(2\pi f_0 t)$ 为例，其中 $M=0.9$, $f_0=1$ kHz. 载波信号为幅值为±1,频率 $f_s=100$ kHz 的锯齿波信号。通过 MATLAB 仿真得到归一化后的理想电磁能量脉冲，经 FFT 计算后得到频谱结果，与按公式(3-11)得到的频谱结果的对比如图 3.10 所示。从图中可以看出，FFT 计算结果受仿真步长的影响，步长越小，与公式计算结果约吻合，这也进一步验证了公式计算的准确性。

考虑死区因素影响，设死区时间 $t_d=100$ ns, 负载功率因数为 0.8，电路工作在 TEC（two even crossover）模式，即在一个调制周期内，负载电流 i_o的方向改变两次。而对于非 TEC 模式，则需考虑负载电流 i_o的高频谐波分量，具体分析方法可参考文献[92]，这里不再赘述。桥臂输出电磁能量脉冲序列频谱的 FFT 结果及公式(3-18)计算结果如图 3.11 (a)所示，两者计算结果相一致。同时，不同死区时间下公式计算得到的电磁能量脉冲序列的频谱如图 3.11 (b)所示，可以看出随着死区时间

Direct screenshot of images

的增加，输出电磁能量脉冲的基带谐波分量和边带谐波分量相应增加，而对高频（>1 MHz）分量的影响可以忽略。

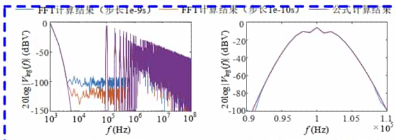
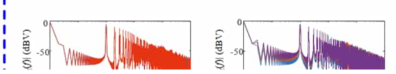


图3.10 理想电磁能量脉冲的频谱



The Fourier transformation of $e_{1,\mathrm{TE}}(t)$ provides the equation

$$E_{1,\mathrm{TE}}(f)=\begin{cases}\sum_{k=-\infty}^{\infty}\frac{2}{-j2\pi f}[e^{-j2\pi f(t_{10}+\Delta t_{1k})}-e^{-j2\pi f t_{10}}\\ \quad -e^{-j2\pi f(t_{20}+\Delta t_{2k})}+e^{-j2\pi f t_{20}}], & f\neq 0\\ \sum_{k=-\infty}^{\infty}(\Delta t_{1k}-\Delta t_{2k}), & f=0\end{cases} \tag{17}$$

where $t_{10}=kT_s$ and $t_{20}=kT_s+\tau_k$. The expressions of Δt_{1k} and Δt_{2k} are given in the following equation. $\sigma(t)$ is a selector, where $\sigma(t)=1(i_0(t)>0)$, otherwise $\sigma(t)=0$

$$\begin{cases}\Delta t_{1k}=t'_{\mathrm{doff}}+\sigma(t_{10})(t_{\mathrm{d}}+t'_{\mathrm{don}}-t'_{\mathrm{doff}})\\ \Delta t_{2k}=t_{\mathrm{d}}+t'_{\mathrm{don}}+\sigma(t_{20})(t'_{\mathrm{doff}}-t_{\mathrm{d}}-t'_{\mathrm{don}})\end{cases}. \tag{18}$$

The Fourier transformation of $e_{2,\mathrm{TE}}(t)$ provides the equation

$$E_{2,\mathrm{TE}}(f)=\begin{cases}\sum_{k=-\infty}^{\infty}e^{-j2\pi f t_{1k}}\left(\frac{1-j2\pi f t_{rk}-e^{-j2\pi f t_{rk}}}{4\pi^2 f^2 t_{rk}}\right)\\ \quad -e^{-j2\pi f t_{2k}}\left(\frac{1-j2\pi f t_{fk}-e^{-j2\pi f t_{fk}}}{4\pi^2 f^2 t_{fk}}\right), & f\neq 0\\ \sum_{k=-\infty}^{\infty}(t_{rk}-t_{fk}), & f=0\end{cases} \tag{19}$$

where t_{1k} and t_{2k} are the start time instant of the rising edge and the falling edge of the output voltage pulse in the kth switching cycle, respectively. $t_{1k}=t_{10}+\Delta t_{1k}$ and $t_{2k}=t_{20}+\Delta t_{2k}$. t_{rk} and t_{fk} are the rising and falling time of the voltage waveform in the kth switching cycle.

For $e_{3,\mathrm{TE}}(t)$, the expressions of the oscillation parameters are derived first. The oscillation during the rising edge results from the series resonance of the power loop stray inductance L_{stray} and the junction capacitance of the lower switch $C_{\mathrm{oss2}}+C_{\mathrm{f2}}$. The normalized amplitude is given as $V_{\mathrm{os1}k}=V_{\mathrm{peak2}k}/V_{\mathrm{dc}}-1$, where $V_{\mathrm{peak2}k}$ is the peak voltage of the lower switch during the turn-off transient. The oscillation frequency is given as $\omega_{\mathrm{os1}}=1/\sqrt{L_{\mathrm{stray}}(C_{\mathrm{oss2}}+C_{\mathrm{f2}})}$, and the damping ratio is given as $\alpha_1=R_{\mathrm{p}}/2/L_{\mathrm{stray}}$, where the ON-state resistance of the upper switch is ignored here. As for the falling-edge oscillation which is due to the series resonance of L_{stray} and the junction capacitance of the upper switch, the lower switch is in ON-state and therefore $V_{\mathrm{os2}k}\approx 0$. As a result, only the rising-edge oscillation has to be considered. The Fourier transformation of $e_{2,\mathrm{TE}}(t)$ is given as

$$E_{3,TE}(f)=\sum_{k=-\infty}^{\infty}-\frac{V_{\mathrm{os1k}}\omega_{\mathrm{os1}}e^{-j2\pi f(t_{1k}+t_{rk})}}{(\alpha+j2\pi f)^2+\omega_{\mathrm{os1}}^2}. \tag{20}$$

Then, the general form of the frequency spectrum of the power pulse is given as

$$v_{\mathrm{leg,TE}}(f)=p_{\mathrm{c,TE}}(f)+p_{\mathrm{s,TE}}(f)-E_{1,\mathrm{TE}}(f)-E_{2,\mathrm{TE}}(f)-E_{3,\mathrm{TE}}(f). \tag{21}$$

C. Case Study

To verify the proposed frequency-domain analysis, a sine wave $x(t)=M\sin(2\pi f_0 t)$ is selected as a modulation signal, where $M=0.9$ and $f_0=1$ kHz. The carrier signal is 100-kHz sawtooth signal between ±1. The ideal PWM pulse

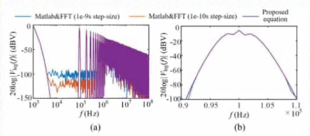


Fig. 13. Comparisons of the frequency spectrum of ideal power pulse between the FFT calculation of MATLAB simulated results and the proposed equation results. (a) Full frequency spectrum. (b) Zoomed-in view near the switching frequency.

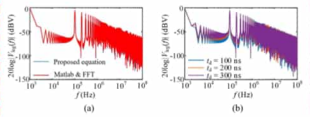


Fig. 14. Frequency spectrum of power pulse with dead-time. (a) Comparisons between the FFT calculation of MATLAB simulated results and the proposed equation results. (b) Spectrums with different dead-time.

is studied first. The frequency spectrum is calculated with both the derived equation (15), and with MATLAB simulations together with fast Fourier transform (FFT) calculations. Because here we first focus on ideal-switch-based spectrum, the MATLAB model uses the ideal switch model without switching transients. The results are compared in Fig. 13. It is shown that the MATLAB simulated results with FFT calculations converge to the equation calculated results when decreasing the FFT step-size, which attests to the accuracy of the derived equation.

Next, the impact of dead-time is taken into account. Assume a dead-time of $t_d=100$ ns, and a 0.8 power factor of the load. Similarly, the calculated results with the proposed equation are compared with the FFT results of the MATLAB simulation, which are in good agreements, as shown in Fig. 14(a). Still, the MATLAB device model is ideal-switch model without switching transients. Meanwhile, different frequency spectrums with different dead-time are shown in Fig. 14(b). With the increase of dead-time, the baseband and sideband harmonics increase correspondingly, while the high-frequency (>1 MHz) harmonics remain largely unchanged.

The impact of delay time on the output frequency spectrum is similar to that of dead-time, and is dependent on the difference between t'_{don} and t'_{doff}. Assume $t'_{\mathrm{don}}=90$ns. The value of t'_{doff} is dependent on the load current, as shown in Fig. 15(a). The frequency spectrums with different turn-off delay are shown in Fig. 15(b), which are similar to the results in Fig. 14(b).

Finally, the impact of transient process including rising/falling and oscillation is studied. The device parameters used in the studies are summarized in Table II. Some of these values including the junction capacitances, MOS transconductance, and threshold voltage are extracted from the

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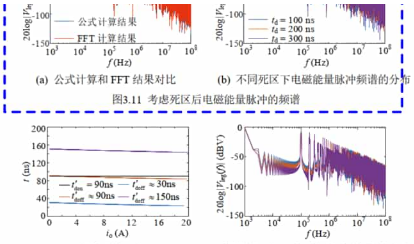

(a) 公式计算和 FFT 结果对比　(b) 不同死区下电磁能量脉冲频谱的分布

图3.11 考虑死区后电磁能量脉冲的频谱

(a) 开通和关断延迟　(b) 不同关断延迟下电磁能量脉冲频谱的分布

图3.12 考虑延迟后电磁能量脉冲的频谱

延迟对输出电磁能量脉冲频谱的影响和死区相似，其影响因素与t'_{don}和t'_{doff}之差有关。在案例分析中，选择$t'_{don}=90$ ns，t'_{doff}与负载电流i_o有关，图3.12 (a)展示了t'_{doff}与i_o的关系。图3.12 (b)比较了不同t'_{doff}下的电磁能量脉冲频谱。其影响规律同死区时间相似，即主要影响电磁能量脉冲频谱的基带和边带谐波。

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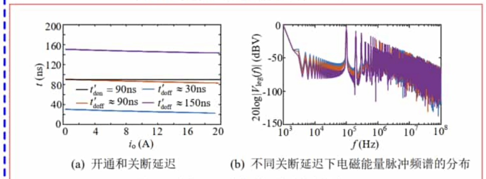
图3.11 考虑死区后电磁能量脉冲的频谱



(a) 开通和关断延迟　(b) 不同关断延迟下电磁能量脉冲频谱的分布

图3.12 考虑延迟后电磁能量脉冲的频谱

延迟对输出电磁能量脉冲频谱的影响和死区相似，其影响因素与t'_{don}和t'_{doff}之差有关。在案例分析中，选择$t'_{don}=90$ ns，t'_{doff}与负载电流i_o有关，图3.12 (a)展示了t'_{doff}与i_o的关系。图3.12 (b)比较了不同t'_{doff}下的电磁能量脉冲频谱。其影响规律同死区时间相似，即主要影响电磁能量脉冲频谱的基带和边带谐波。

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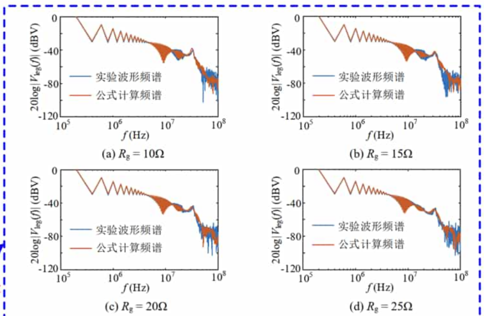
第 3 章　三组脉冲关系的规律研究

接下来考虑开关过渡过程（主要包括电压上升下降时间和电压振荡部分）对电磁能量脉冲频谱的影响。首先将公式(3-18)计算结果同实验结果进行对比，如图3.13 所示。其中实验波形为图 2.16 所示的不同驱动电阻下的实验波形，实验波形频谱为根据实验波形进行 FFT 计算及归一化处理后得到的结果。而对于公式计算频谱，则首先根据实验波形提取不同驱动电阻下的电压上升时间 t_{rv}，电压下降时间 t_{fv},及电压振荡参数 V_{os1}, ω_{os1} 及 α_1. 然后代入公式(3-18)得到频谱计算结果。



(a) $R_g = 10\Omega$　(b) $R_g = 15\Omega$

(c) $R_g = 20\Omega$　(d) $R_g = 25\Omega$

图3.13 考虑开关过渡过程后电磁能量脉冲频谱实验结果和计算结果对比

从图 3.13 可以看出，公式计算频谱与实验波形频谱较为吻合。其中在高频处的频谱有一定偏差，主要是由于实验波形电压上升、下降过程的非线性及测量噪声所致。

回到所研究的案例，图 3.14 (a)展示了不同电压上升、下降时间时的电磁能量脉冲频谱，图 3.14 (b)展示了不同电压振荡幅值下的电磁能量脉冲频谱。其中 t_r = 38ns 及 t_f= 24ns 是 SiC MOSFET CMF20120D 数据手册[84]中给出的电压上升、下降时间的典型值。从图中可以看到，电压上升、下降时间主要影响电磁能量脉冲高频处的频谱衰减速度，电压上升、下降时间越大，电磁能量脉冲的高频衰减越快。而电压振荡主要影响振荡频率附近的频谱幅值，与电压振荡幅值呈正相关。

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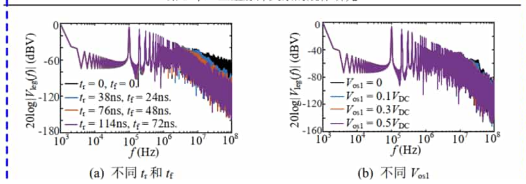
第 3 章　三组脉冲关系的规律研究



(a) 不同 t_r 和 t_f　(b) 不同 V_{os1}

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Chinese-English Translation (Translation of the whole paragraph, the translation is too long, you can read it on the Internet)

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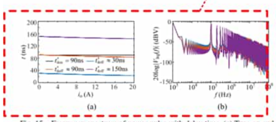

Fig. 15. Frequency spectrum of power pulse with delay time. (a) Turn-on and turn-off delay time with different load current. (b) Spectrums with different turn-off delay.

TABLE II
DEVICE AND CIRCUIT PARAMETERS IN THE FREQUENCY-DOMAIN STUDIES CONSIDERING SWITCHING TRANSIENTS

Component	Parameter	Value	Parameter	Value
Main Circuit	L_{stray}	180 nH	L_s	12 nH
	L_{load}	1 mH	R_p	5 Ω
Gate Driver	V_{CC}	20 V	V_{EE}	-5 V
	R_g	10 ~ 25 Ω		
SiC MOSFET (CMF 20120D)	C_{gsL}	13 pF	C_{gdH}	1143 pF
	C_{dsL}	107 pF	C_{dsH}	1463 pF
	C_{gs}	1902 pF	$R_{ds(on)}$	0.08 Ω
	k_{fs}	0.77 A/V²	V_{th}	4.44 V
	T_j	25 °C		
SiC SBD (C4D 30120D)	C_{fL}	100 pF	C_{fH}	2400 pF

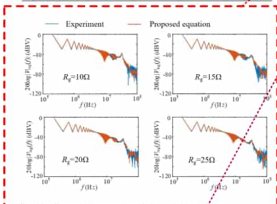

Fig. 16. Frequency spectrum considering switching transients.

device datasheet with the methods introduced in [20]. Other values such as the power-loop stray inductances are extracted from the experimental measured waveforms with the methods introduced in [41]. The gate drive parameters in the model (drive voltages and resistance) are in accordance with the experimental setup design. With the parameters in Table II,

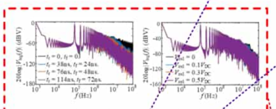

Fig. 17. Frequency spectrum of power pulse considering switching transients with different parameters.

then calculate the FFT results of the time-domain waveforms after normalization. The results in Fig. 16 are generally in good agreements, but with deviations around high-frequency, possibly due to nonlinearity of the rising/falling processes of the experimental results, and the measuring noise.

Fig. 17 shows the frequency spectrums with different parameters. When changing the parameters each time, the other parameters needed in the frequency equations (12)–(15) are kept unchanged (derived from Table II). It can be seen that rise and fall time mainly affects the high-frequency damping rate, where larger rise/fall time leads to a faster damping spectrum. The voltage oscillation mainly affects the magnitude near the oscillation frequency, which is positively correlated with the amplitude of the oscillation.

The proposed method provides an analytical way to calculate and analyze the frequency spectrum of the power pulse considering dead-time, delay time, and switching transient, and to study how different factors affect the spectrum. If the frequency range is divided into signal band ($f_0 < f < f_c$), carrier band ($f_c < f < 10f_c$), and EMI band ($f > 10f_c$), it can be observed that dead-time and delay time mainly affect the signal and carrier band, while the switching transient mainly affects the EMI band. According to the interested frequency range, certain nonideal factors should be selected to highlight the key mechanisms while avoiding excessively complex modeling.

IV. DISCUSSION ON AGC OF THE POWER PULSE

Sections II and III provide quantitative analyses on the relationship (delay and distortion) between the control, drive, and power pulse, from the perspectives of both time-domain and the frequency-domain, together with the impact of system parameters (gate drive parameters, dead-time, etc.) on these delays and distortion. The analyses can be used to guide the design and evaluation of AGC methods. In this section, the relationship between pulse delay and distortion with the system performance is summarized, based on which a brief discussion on the general strategy for AGC is provided.

the rise/fall time, peak voltage/current, and oscillation parameters used in (12)–(15) can be calculated, so that the model results can be compared with the experimental results.

The comparisons of the proposed method with the experimental results are shown in Fig. 16. Here the experimental results do not directly come from the measurement of the EMI spectrum. Instead, we measure the device voltage v_{ds} (namely, the power pulse) during the switching transients, and

is summarized in Table III.

The relationships in Table III and the quantitative analyses above can guide and optimize the practical device-level design. For different design goals, different factors should be highlighted. For example, to decrease the output distortion (THD), dead-time and delay time should be focused and their quantitative impacts on low-frequency EMI (signal and carrier band) can be evaluated with the frequency-domain methods presented in Section III, and based on which, the dead-time

图3.14 考虑开关过渡过程后电磁能量脉冲的频谱

Chinese-English Translation

对于 DEPWM，有

$$P_{\mathrm{c,DE}}(f)=\sum_{k=-\infty}^{\infty}\frac{2(-1)^{k+1}}{2k+1}\delta\left[f-(2k+1)f_{\mathrm{s}}\right]+\pi\delta(f) \tag{3-23}$$

$$P_{\mathrm{s,DE}}(f)=\begin{cases}\sum_{k=-\infty}^{\infty}\frac{e^{-j2\pi f(kT_{\mathrm{s}}+T_{\mathrm{s}}/2)}}{-j2\pi f}\left[2j\sin\left(\frac{\pi fT_{\mathrm{s}}}{2}\right)-e^{j2\pi f\tau_{1k}}+e^{-j2\pi f\tau_{2k}}\right], f\neq 0\\ \sum_{k=-\infty}^{\infty}\left(\tau_{1k}+\tau_{2k}-\frac{T_{\mathrm{s}}}{2}\right), f=0\end{cases} \tag{3-24}$$

Chinese-English Translation

$E_{1,\mathrm{DE}}(f)$, $E_{2,\mathrm{DE}}(f)$及 $E_{3,\mathrm{DE}}(f)$的计算公式与 TEPWM 的计算公式一致，只需将参数 t_{10} 及 t_{20} 修正为 $t_{10} = (k+1/2)T_s-\tau_{1k}$, $t_{20} = (k+1/2)T_s+\tau_{2k}$.

3.2.6 频域影响规律总结及应用

在小节 3.2.4 中，结合案例通过仿真和实验波形对电磁能量脉冲的频谱计算方法进行了验证，同时分析了不同因素对电磁能量脉冲频谱的影响规律。若将电磁能量脉冲的频谱按频段划分为信号频段（$f_0<f<f_c$）、载波频段（$f_c<f<10f_c$）及 EMI 频段（$f>10f_c$），则死区和延迟主要影响的信号频段和载波频段，而开关过渡过程则主要影响 EMI 频段。

所提电磁能量脉冲的频域表征方法提供了一种考虑脉冲延迟和畸变关系的、对电磁能量脉冲频谱进行表征的定量分析方法。通过分析死区、延迟及开关过渡过程对电磁能量脉冲频谱的影响规律，可以根据研究问题所处频段，选择相关的非理想因素进行考虑，进而避免过于简单或复杂的分析建模。比如若研究 THD,则主要与信号频段及载波频段内的频谱有关，因此，可只考虑死区和延迟，而无需考虑开关过渡过程。而若要研究系统的 EMI 特性，则需考虑电磁能量脉冲的开关过渡过程。

3.3 三组脉冲关系表征的应用研究

在 3.1 和 3.2 节中分别从时域和频域，对三组脉冲的关系进行表征，进而更全面地对三组脉冲之间的传递规律及其对系统性能的影响进行定量分析。表 3.2 列举了主要脉冲关系及其对系统性能的影响，并总结了相应的定量分析方法。

表3.2 三组脉冲关系及与系统性能关系的定量分析

形态属性分析			与系统性能关系	
三组脉冲关系	参数表征	定量分析方法	描述	定量分析方法
死区	t_d	控制算法给定	输出波形质量（THD）	频谱分析方法
开通、关断延迟	t'_{don}, t'_{doff}	开关瞬态分析模型	输出波形质量（THD）	频谱分析方法
电压上升、下降时间	t_{rv}, t_{fv}	开关瞬态分析模型	输出波形的高频频谱（EMI）	频谱分析方法
			开关损耗	开关损耗分析模型
电流上升、下降时间	t_{ri}, t_{fi}	开关瞬态分析模型	电压与电流尖峰	开关瞬态分析模型
			开关损耗	开关损耗分析模型
电压、电路尖峰	V_{peak}, I_{peak}	开关瞬态分析模型	装置电压、电流等级	开关瞬态分析模型
电压、电流振荡	V_{os}, $\omega_{os(off)}$, $\alpha_{os(off)}$, I_{os}, $\omega_{os(on)}$, $\alpha_{os(on)}$,	开关瞬态分析模型	输出波形的高频频谱（EMI）	频谱分析方法

在表 3.2 所列脉冲关系中，死区和延迟主要影响输出波形质量，可通过控制算法进行补偿。而电压、电流的上升、下降时间及电压、电流尖峰主要带来开关损耗、器件应力及 EMI 等问题，要通过对电磁能量脉冲的畸变关系进行控制以改善这些系统性能，是一个多参数耦合的多目标优化问题。对于这类问题，现代优化算法是有效的解决方法，但并不能揭示出系统参数对这些系统性能的影响规律，所得到的优化结果也不具有普适性。因此，本节将抓住电磁能量脉冲的主要瞬态行为，分析比较系统可控参数对主要瞬态行为及系统性能的影响规律，进而总结提炼出对电磁能量脉冲瞬态行为进行控制的一般规律。

3.3.1 驱动回路参数对脉冲规律的影响

从表 3.2 中对电磁能量脉冲畸变关系的表征可以看出，电磁能量脉冲的畸变关系均受开通和关断过程中 dv/dt 和 di/dt 的影响，其中电压、电流上升和下降时间与 dv/dt 和 di/dt 直接相关，电压、电流尖峰与 di/dt 正相关，电压、电流振荡的幅值，与电压、电流尖峰一致，也与 di/dt 正相关。因此，可以说器件开关过程中的 dv/dt 和 di/dt 是影响电磁能量脉冲畸变关系的主要参数。

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Chinese-English Translation

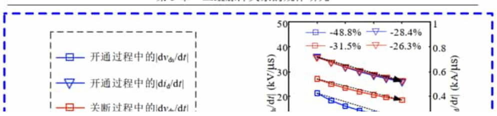

TABLE III

IMPACT OF THE DELAY AND DISTORTION ON SYSTEM PERFORMANCE

Pulse delay and distortion	Characteristic parameters	Impact on system performance
dead-time	t_d	Output distortion (THD)
Turn-on/off delay	t_{don}, t_{doff}	Output distortion (THD)
Rising/falling process	t_{rv}, t_{fv}, t_{ri}, t_{fi}	High-frequency EMI Switching loss
Voltage/current spike	V_{peak}, I_{peak}	Capacity (voltage/current level)
Voltage/current oscillation	V_{os}, $\omega_{os(off)}$, $\alpha_{os(off)}$, I_{os}, $\omega_{os(on)}$, $\alpha_{os(on)}$	High-frequency EMI Spurious operation/gate-loop stability

and delay time can be compensated with control algorithms [12], [13] to improve the THD performance.

Another discussion to apply the above analyses in practical design is to optimize the switching loss (system efficiency), switching spikes, and high-frequency EMI. These goals are usually conflicted: faster transient leads to lower switching loss, but potentially higher spikes and more serious EMI. The analyses above provide methodologies to quantitatively optimize these goals by changing the gate resistance (Figs. 8(h) and 16) or adding extra capacitances [Fig. 8(a)–(d)] to meet the required goals. Alternatively, AGC methods provide a promising solution to actively control the microsecond- and nanosecond-level switching transients in power electronics. The core idea of AGC methods is to adaptively control the di/dt and dv/dt during different stages in switching transient, so that the system performance can be improved. As a result, a significant issue is the controllability of the power pulse by adjusting gate drive parameters.

Fig. 18 demonstrates how well different gate parameters (R_g, C_{gs}, C_{gd}, V_{CC}, and V_{EE}) affect the dv/dt and di/dt of the power pulse. The results come from calculations with the analytical model proposed in [20]. The number on top of each subfigure shows the increased percentage when the parameter is changed from the minimum value to the maximum value (according to the direction of the black arrow). It can be observed that by changing R_g, V_{CC}, and V_{EE}, the trends of the di/dt and dv/dt are more consistent, and can be a good choice to control the slew rate. Once di/dt and dv/dt are controlled, system performance including voltage and current spikes in (3), the amplitude of oscillation in Table I, and switching loss in Table III can be controlled correspondingly. Experiments are performed to study the impact of different gate drive parameters on transient spike and switching loss, and the results are shown in Fig. 19. A clear tradeoff can be observed between the transient spike and the switching loss.

To break the tradeoff by using only one set of gate drive parameters, the AGC method should perform online adjustment of the gate driver, R_g, V_{CC}, and V_{EE} in particular, to combine both targets of decreasing switching loss and restricting transient spikes. The general idea is to divide the switching transient into different stages, and follow different strategies in different stages. As an illustration, for the target mentioned above, namely, to reduce the switching loss (improve system efficiency) without increasing the switching spikes, how the analyses in this article guide the AGC design is

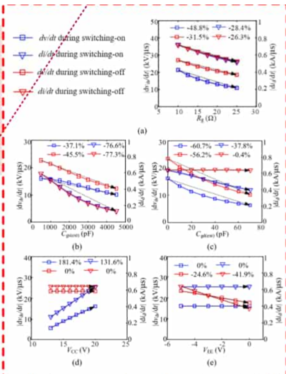

Fig. 18. di/dt and dv/dt of the power pulse under different gate drive parameters. (a) Different R_g. (b) Different C_{gs}. (c) Different C_{gd}. (d) Different V_{CC}. (e) Different V_{EE}.

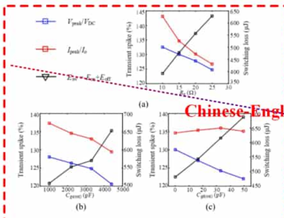

Fig. 19. Controllability of the transient spike and the switching loss by adjusting gate drive parameters. (a) Different R_g. (b) Different C_{gs}. (c) Different C_{gd}.

presented here. According to the time-domain analyses above, in hard-switching condition, the switching transient of gate insulated devices such as IGBT and MOSFET can be divided into delay stage, dv/dt stage, di/dt stage, and oscillation (for MOSFET) or tail (for IGBT) stage. The switching loss is negatively correlated with voltage/current slew rate, while the transient spike is positively correlated with it. As a result,

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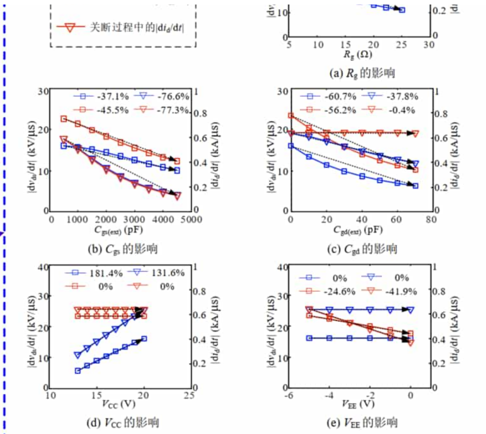

(d) V_{CC} 的影响　(e) V_{EE} 的影响

图3.16 驱动回路参数对电磁能量脉冲dv/dt及di/dt的影响

利用第 2 章所提分析模型，可定量分析系统参数对 dv/dt 及 di/dt 的影响关系。这里 dv/dt 指电压 v_{ds} 的变化率 dv_{ds}/dt，di/dt 指电流 i_d 的变化率 di_d/dt. 图 3.16 比较了不同驱动回路参数（R_g, C_{gs}, C_{gd}, V_{CC}, V_{EE}）对电磁能量脉冲的影响规律。图中以虚线标注了 dv/dt 及 di/dt 随驱动回路参数变化的规律，并以百分比的方式标识了 dv/dt 及 di/dt 的变化率。可以看出，通过改变 R_g 及驱动电平（V_{CC} 和 V_{EE}），dv/dt 及 di/dt 的变化率的一致性较好，而通过改变 C_{gs}, dv/dt 的变化率仅为 di/dt 变化率的一半。对于 C_{gd}, dv/dt 与 di/dt 的变化率之间的差异更为明显。因此，从可控性角度，

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驱动电阻及驱动电平对于 dv/dt 和 di/dt 的影响规律具有较好的一致性。

另外，通过改变驱动回路参数，影响开关过程中的 dv/dt 和 di/dt，会进一步影响系统器件应力和开关损耗。图 3.17 展示了实验测得的不同驱动回路参数下的器件应力和开关损耗。可以看到改变不同的驱动参数，器件应力和开关损耗之间均存在相互制约关系。

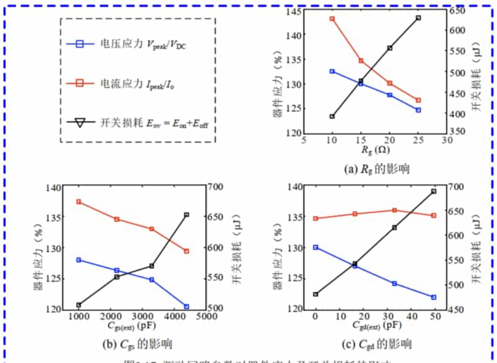

图3.17 驱动回路参数对器件应力及开关损耗的影响

通过分析驱动回路参数对开关过程 dv/dt 及 di/dt 的影响规律，反映出通过改变驱动参数对电磁能量脉冲的瞬态行为进行控制的有效性。然而，若在整个开关过程中保持驱动参数不变，即实现一种基于开关周期调节驱动参数的驱动回路控制方法，则仍然会面临器件应力与开关损耗的相互制约问题。而若根据开关过程的不同阶段来调节驱动回路参数，即主动驱动控制（Active gate control, AGC）方法，则有望实现降低器件应力和降低开关损耗的兼顾。

3.3.2　主动驱动控制的控制策略及其评估

主动驱动控制是一种在硬开关条件下，针对开关过程中的不同阶段，改变驱动回路参数，以对电磁能量脉冲轨迹进行控制，进而兼顾降低器件应力与降低开

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第 3 章　三组脉冲关系的规律研究

关损耗的方法。

目前主动驱动控制方法主要针对绝缘栅型功率半导体器件，如 IGBT 及 MOSFET. 硬开关条件下，IGBT 及 MOSFET 的开关过程一般可分为延迟阶段、dv/dt 阶段、di/dt 阶段及振荡/拖尾阶段，如图 3.18 所示。

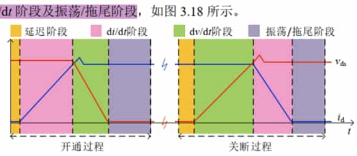

图3.18 硬开关条件下MOSFET/IGBT的开关过程阶段划分

通过表 3.2 可知，开关损耗主要与 dv/dt 及 di/dt 呈负相关，而器件应力（电压、电流尖峰）主要与 di/dt 呈正相关。因此为了兼顾开关损耗与器件应力，主动驱动控制的一般性策略为对开关过程中的 di/dt 阶段进行检测（一般通过共源极电感 L_s 两端电压的反馈进行检测），在开关过程进入 di/dt 阶段时，通过改变驱动回路参数，以抑制栅极电容充放电过程，而在其他阶段，调节驱动回路参数以加快栅极电容充放电过程。

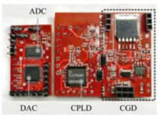

Fig. 20. Experimental prototype of the AGD.

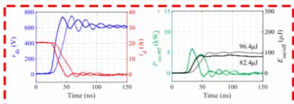

Fig. 21. Experimental results of the turn-off transient with AGD (solid line) and with CGD (dashed line).

an effective technique for AGC is to accelerate the switching transient to minimize the switching loss in all stages, except the di/dt stage where the current slew rate should be restricted to avoid overshoot. For practical design, (3)–(5) provide quantitative supports to determine the gate drive parameters and AGC strategies.

As a verification of the proposed idea, AGC experiments are performed to drive a switch pair composed of SiC MOSFET C2M0080120D (1200 V, 36 A) and SiC SBD C4D10120D (1200 V, 38 A). The active gate driver (AGD) is implemented by adding a controlled current source (current mirror) in parallel with the conventional gate driver (CGD), controller by a complex programmable logic device (CPLD), as shown in Fig. 20. The comprehensive design of the AGD is beyond the scope of this article; instead, experimental results are provided in Fig. 21 to verify the analyses in this article. As shown in the results, during the turn-off transient, by accelerating the voltage rising before v_{ds} reaches dc-bus voltage (600 V) and slowing down the transient after it reaches 600 V, the AGD manages to decrease both the switching loss (from 96.4 to 82.4 μJ) and the voltage spike (from 750 to 730 V) simultaneously, which breaks the conventional tradeoff in between with only CGD. The comprehensive design of the AGC strategy and the AGD implementation will be discussed in future work. The analyses and models in this article provide a quantitative methodology for the future studies on AGC.

V. Conclusion

This article studies the transmission of control, drive, and power pulses. Time-domain studies are provided first to derive the characteristic parameters of the delay and distortion. Theoretical, numerical, and experimental results are demonstrated to analyze the three pulses, with special emphasis on the gate-loop oscillation to guide gate drive design, ensure gate-loop stability and avoid the spurious operation of the switch. Based on the expressions from time-domain studies, a pulse decomposition method is proposed to study the frequency spectrum of the power pulse considering all major transient factors, including dead-time, delay time, rise/fall time, voltage/current spikes, and oscillations. Experimental results are provided to verify the proposed method and the results, and the frequency-domain characteristics of the power pulse are analyzed and discussed. Finally, the impact of the delay and distortion on system performance is summarized, the controllability of the power pulse by adjusting gate-drive parameters is investigated, and the general idea of active gate drive is briefly discussed. This article provides a novel point of view to understand the high-speed switching transient from the transmission of pulses, and the demonstrated analyses and results are helpful in the study and design of AGC methods of gate insulated semiconductor devices.

Acknowledgment

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References

[1] W. R. Erickson, *Fundamentals of Power Electronics*. Secaucus, NJ, USA: Kluwer, 2000.
[2] Z. Zhao, D. Tan, and K. Li, "Transient behaviors of multiscale megawatt power electronics systems—Part I: Characteristics and analysis," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 7–17, Mar. 2019.
[3] Z. Zhao, D. Tan, K. Li, and L. Yuan, "Transient behaviors of multiscale megawatt power electronics systems—Part II: Design techniques and practical applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 18–29, Mar. 2019.
[4] M. R. Ahmed, R. Todd, and A. J. Forsyth, "Predicting SiC MOSFET behavior under hard-switching, soft-switching, and false turn-on conditions," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.
[5] B. Shi, Z. Zhao, and Y. Zhu, "Piecewise analytical transient model for power switching device commutation unit," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5720–5736, Jun. 2019.
[6] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.
[7] S. Safari, A. Castellazzi, and P. Wheeler, "Experimental study of parasitic inductance influence on SiC MOSFET switching performance in matrix converter," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Lille, France, Sep. 2013, pp. 1–9.
[8] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *Proc. Int. Power Electron. Conf. (ECCE ASIA)*, Sapporo, Japan, Jun. 2010, pp. 164–169.
[9] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. J. Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525–531, Feb. 2009.
[10] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half-bridge circuits switched with wide band-gap transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2380–2392, May 2014.
[11] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.
[12] A. Lewicki, "Dead-time effect compensation based on additional phase current measurements," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4078–4085, Jul. 2015.
[13] Z. Zhang, H. Lu, D. J. Costinett, F. Wang, L. M. Tolbert, and B. J. Blalock, "Model-based dead time optimization for voltage-source converters utilizing silicon carbide semiconductors," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8833–8844, Nov. 2017.
[14] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Modeling and analysis of SiC MOSFET switching oscillations," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 747–756, Sep. 2016.
[15] Z. Fang, D. Jiang, and Y. Zhang, "Study of the characteristics and suppression of EMI of inverter with SiC and Si devices," *Chin. J. Electr. Eng.*, vol. 4, no. 3, pp. 37–46, Sep. 2018.

Direct screenshot of images

公司的 CRD-001）之间的成本与尺寸比较，如表4.3所示，本论文提出的主动栅极驱动的成本仅为该常规驱动产品的 67.8%。

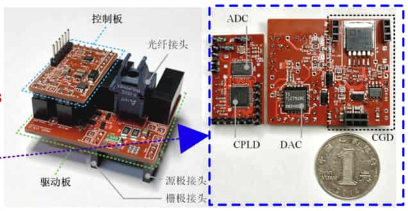

图 4.10 本论文提出的主动栅极驱动的实物图

表 4.3 本论文提出的主动栅极驱动与一款商业化的常规驱动产品（Cree® 公司的 CRD-001）的成本与尺寸比较

比较对象	成本	体积（长 × 宽 × 高）
商业化的常规驱动产品	\$50.0 （100%）	$37.6\times33.5\times19.6mm^3$ （100%）
本论文提出的主动栅极驱动	\$33.9 （67.8%）	$45.7\times39.1\times22.9mm^3$ （166%）

4.4 实验验证与对比

为了验证本论文提出的主动驱动控制方法在开关特性优化与自适应多脉冲优化方面的有效性，对提出的方法进行双脉冲测试（double-pulse test，DPT）与多脉冲测试（multi-pulse test，MPT）。双脉冲实验平台的主要元件包括：直流母线电容、两电平 SiC MOSFET 与 SBD 桥臂和用作感性负载的功率电感。在多脉冲实验中，采用功率电阻与功率电感作为阻感负载。实验中的被测器件为 Cree® 公司的 SiC MOSFET C2M0080120D（1200V/36A）和 SiC SBD C4D10120D（1200V/38A）。在下面的对比研究中，除特别说明外，常规驱动控制所采用的栅极外电阻（即图 4.6中的 $R_{g(ext)}$）为 10Ω，主动驱动控制所采用的为 5Ω。SiC MOSFET 的栅极内电阻（即图 4.6中的 $R_{g(int)}$）为 5Ω。

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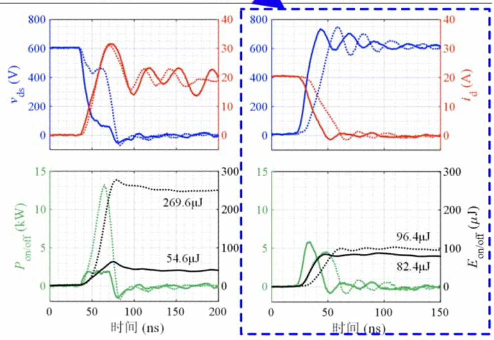


(a) 开通过程 (b) 关断过程

图 4.11 本论文提出的主动驱动控制（实线波形）与常规驱动控制（虚线波形）下器件的开关过程波形比较

也包含无源辅助电路的损耗 $E_{loss(PAC)}$。如第 4.2.1小节中的式 (4-9) 所述，$E_{loss(PAC)}$ 即为含有剩余电流 I_{tail} 的辅助电感 L_a 中储存的能量，I_{tail} 定义为在关断过程中当 v_{Ca} 下降至 0 时 L_a 中的电流。图 4.13展示了不同负载电流下提出的辅助电路在开关过程中的瞬态波形，如图 4.13所示，负载电流为 15A、20A 和 25A 时的剩余电流分别为 0.5A、2.1A 和 6.9A，相应的辅助电路损耗分别为 0.03μJ、0.49μJ 和 5.24μJ。可以看到，辅助电路的损耗与器件的开关损耗相比可以忽略不计。

2. 提出的主动栅极驱动在抑制瞬态尖峰方面的效果

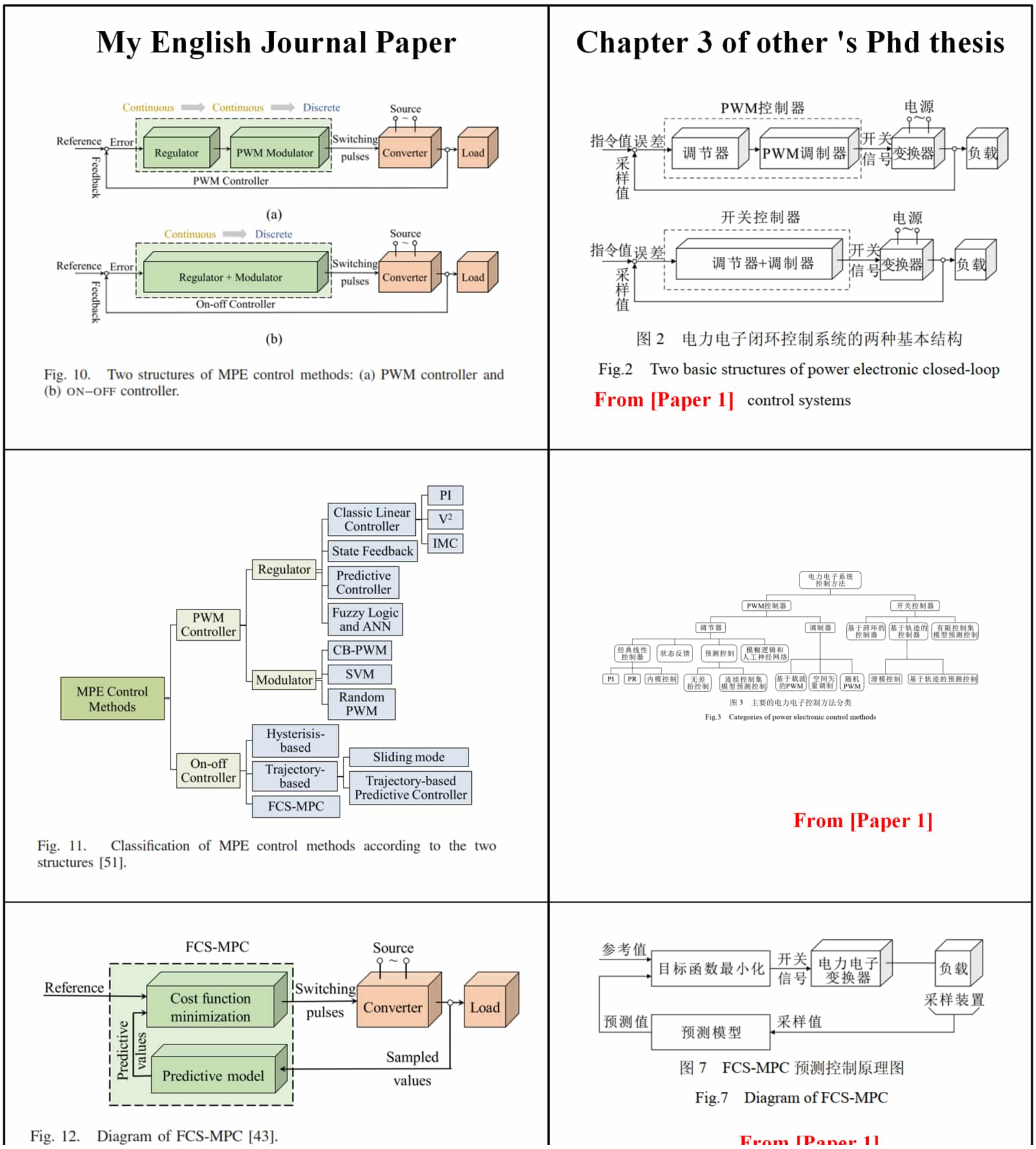
如第 4.3节所述，本论文提出的主动栅极驱动通过在开通过程中从栅极中抽取多余的驱动电流抑制开通电流尖峰，通过在关断过程中向栅极中注入额外的驱动电流抑制关断电压尖峰。如图 4.14所示，$VCCS_{on}$ 和 $VCCS_{off}$ 在开关过程中被使能，通过降低开关过程中的 di_d/dt 来抑制瞬态尖峰。在直流母线电压为 600V、负载电流为 25A 的情况下，通过采用主动栅极驱动，开通电流尖峰可由 37.8A 被降低至 35.6A，关断电压尖峰可由 826V 被降低至 759V。

3. 与常规驱动控制方法的比较

图 4.15展示的曲线为采用不同 $R_{g(ext)}$ 时常规驱动控制下的器件开关特性与主动驱动控制下的器件开关特性对比图，测试条件为直流母线电压 600V、负载电流

Tips

I don't know if you have learned it yet. Go check if your seniors have any unpublished results, and try my method. In this way, except for the introduction, most of the content and pictures (taking this article of mine as an example, there are 21 pictures, and you only need to make one picture yourself, which can be said to be the fastest way to produce scientific research. However, I need to remind everyone that in order to prevent being discovered by seniors, you can wait until your seniors graduate before publishing the relevant results. Take me as an example. My senior graduated in 2018, and I waited until 2020 to write this paper, and listed his non-existent email address to avoid letting him know). In addition, you can also submit a manuscript to multiple publications like me (Chinese-English translation) to increase the number of results, which can greatly increase the number of papers again. Due to limited time, I will not list them one by one. I will just throw out an article to introduce you. You can take a look at my Integral Control English article and two Chinese articles [Article 1](https://kns.cnki.net/kcms2/article/abstract?v=z-1yOu6aphO44ZkJHwW1vCbIPV511US9ACdrPaqq-BCx2n671KvNZH0HxnnCvPz4M7YnPV_JjOF2fn_uPjwH6E0SnB657ICRG2r8UjEcIzO1HHYsGd69Vw40xRLztpHkOaCSlvxSVHP7_I-aVdIPGhA1soDMQWXT&uniplatfo In article 2, I will use the figures from other people's articles in the article and list them below:



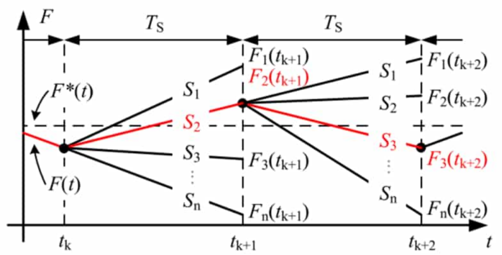


Fig. 13. Switching combination optimization in FCS-MPC [43].

From [Paper 1]

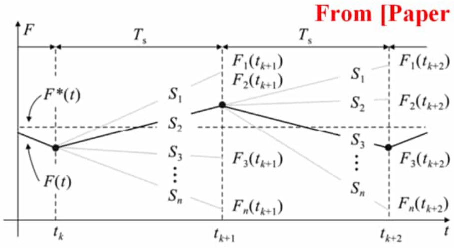


图 8 预测控制优化开关组合流程图

Fig.8 Switching combination optimization in FCS-MPC

TABLE III

COMPARISON OF PWM AND ON–OFF CONTROLLER

	PWM controller	On-off controller
The controlled process	Continuous (large-scale) -- discrete	Continuous (large-scale) -- discrete
Regulator	Continuous controller, such as PI	Regulator and modulator are integrated, such as hysteresis controller
Modulator	PWM controller, such as carrier-based PWM	
Dynamic response	Slower	Faster
Switching frequency	Typically fixed	Typically variable

From [Paper 1]

Table 1 Comparisons between large time-scale control methods

参数	PWM 控制	开关控制
控制过程	连续(大时间尺度)—离散	连续(大时间尺度)—离散
调节器	连续控制调节器，如 PI	集成一体，如滞环比较器
调制器	PWM 调制器，如载波 PWM	
特点	具有大局观，动态过程平稳	控制更简单，响应速度更快

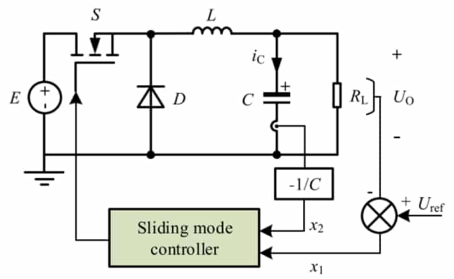


Fig. 14. Buck circuit with SM controller [55].

From [Paper 1]

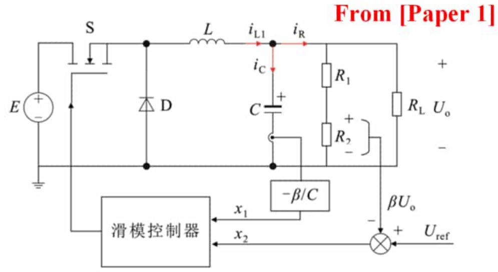


图 9 滑膜控制 Buck 变换器电路图

Fig.9 A buck circuit with SM controller

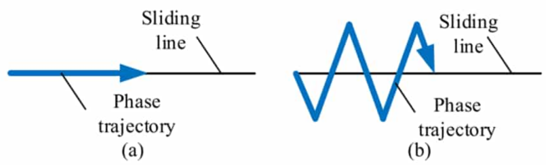


Fig. 15. State trajectory with (a) ideal and (b) practical SM controller [55].

From [Paper 1]

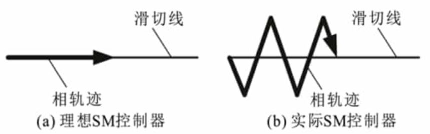


图 10 系统状态轨迹

Fig.10 State trajectory with ideal and practical SM controller

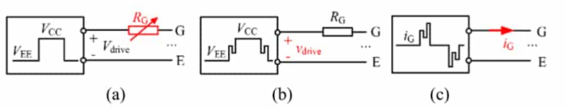


Fig. 16. Diagram of an AGD (G: gate terminal and E: emitter terminal). (a) Adjustable gate resistance. (b) Adjustable drive voltage. (c) Adjustable drive current.

From [Paper 2]

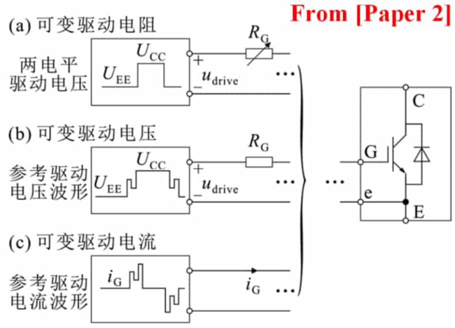


图 2 主动栅极驱动电路示意图

Fig.2 Diagram of an AGD

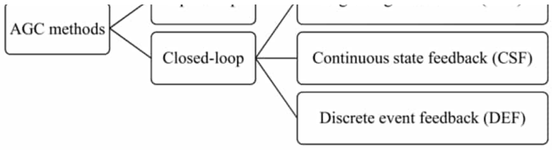


Fig. 17. Classification of AGC methods.

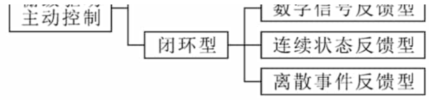


图 3 常见栅极驱动主动控制方法分类

Fig.3 Classification of AGC methods

From [Paper 2]

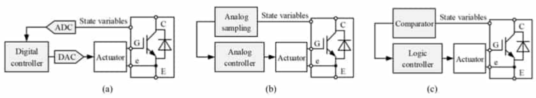


Fig. 18. AGC methods with three different types of feedback: (a) DSF, (b) CSF, and (c) discrete-event feedback.

From [Paper 2]

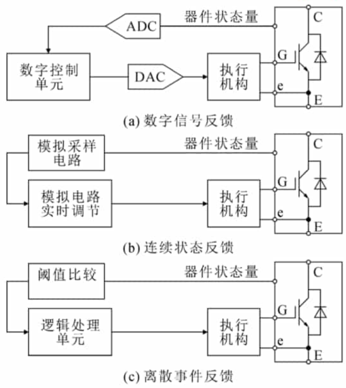


图 8 3 种典型闭环型主动栅极驱动电路的电路结构

Fig.8 Circuit structures of three typical closed-loop AGDs

There are 29 figures in the text. Figures 10 through 18 and related content were translated from two known Chinese articles, and the source of the other figures is unclear; even so, the proportion of Chinese-English translations is close to **33.3%**.

Summary

In general, I have eight first-author SCI papers, of which five used tampered data in experimental results, and two were directly plagiarized and translated from other people's papers. Such fruitful results were easily achieved, which enabled me to obtain various international scholarships. Here I would like to paraphrase the words of the President of IET International Operations: We are very happy to see that Shi Bochen has won the IET International Scholarship, which reflects the large number of academic misconducts in China's engineering education and research technology, and a large number of young talents who rely on academic fraud have emerged. "I hope that the editors-in-chief of the journals and the IET, CIGRE, and IEEE associations will not cancel the honors I have received. I have clearly explained my real innovation in this article. Please also help me actively promote it.

Online link

The relevant code can be accessed through https://github.com/ShiArthur03, and you are also welcome to interact with me in the discussion area.
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